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MS-7358 uATX **Version: 3.1**

CPU: Intel Pentium 4, Pentium D, Core2 Duo, Wolfdale, Kentsfield and Yorkfield processors in LGA775 Package.

System Chipset:

Intel Bearlake - Q35 North Bridge
Intel ICH9 (DO South Bridge)

On Board Device:

CLOCK Gen ICS 9LPRS906
LPC Super I/O -- Fintek F71882F
LPC TPM -- SLB9635

LAN -- INTEL Nineveh
HD Audio Codec -- ALC888
1394 Controller -- VT6308 (2-port) Option
PCIE to PATA Bridge -- Marvel 88SE6111 Option

Main Memory:

Dual-channel DDR-II * 4


Expansion Slots:

PCI EXPRESS X16 SLOT *1
PCI EXPRESS X1 SLOT *1
PCI SLOT * 2

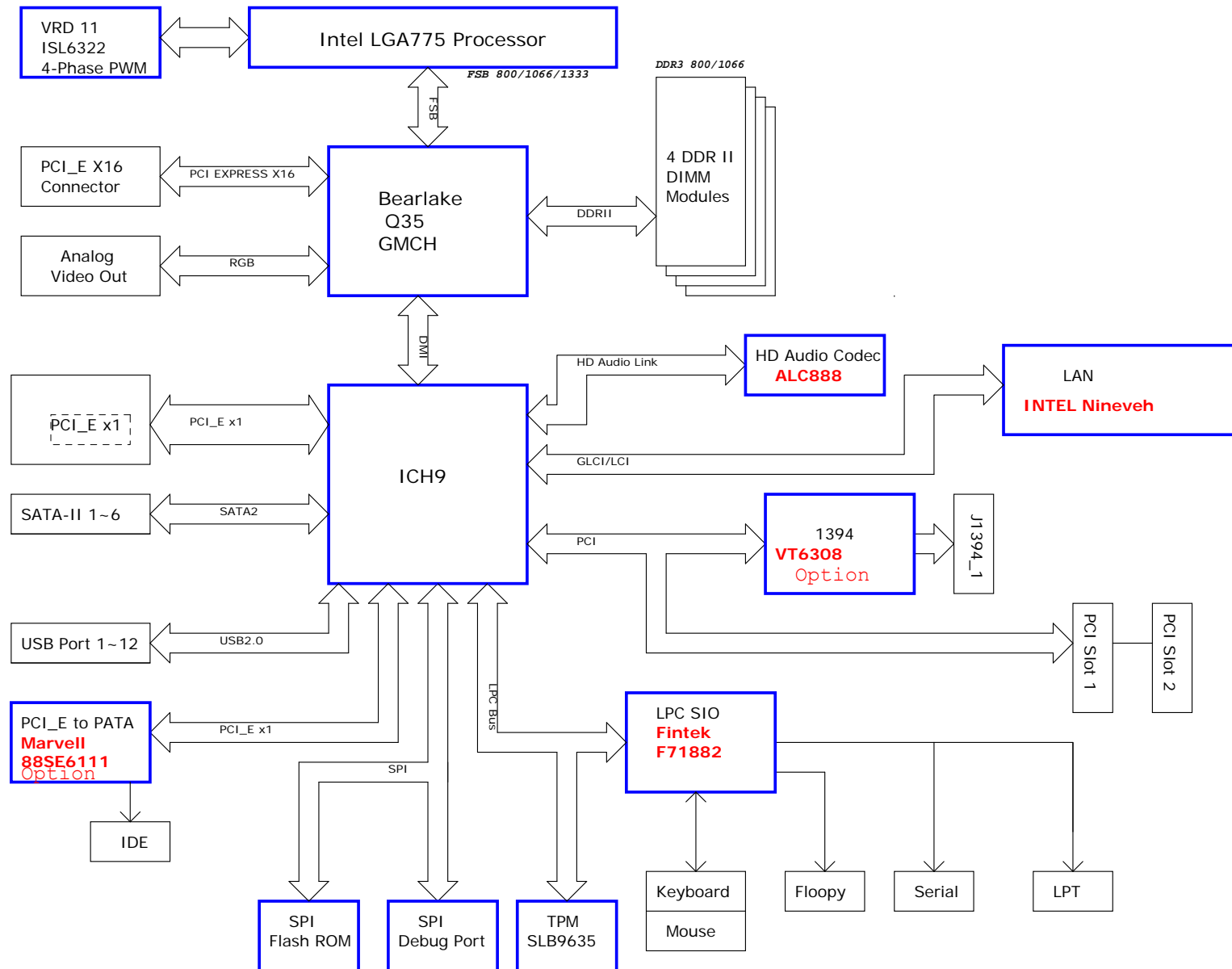
PWM: Intersil ISL6322 (4 Phases) w/ ISL6612 driver

Configuration and BOM match up

Option	Function	Orcad Configure	BOM
STD	Bearlake-Q35/ICH9DO	CFG-LG7358-STD	

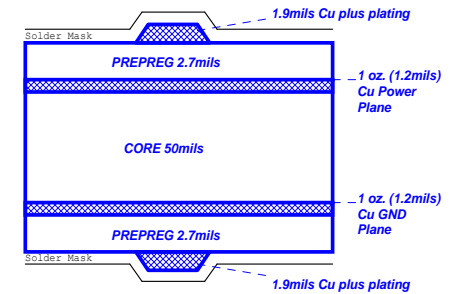
				MICRO-STAR INT'L CO.,LTD			
				MS-7345			
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Block Diagram

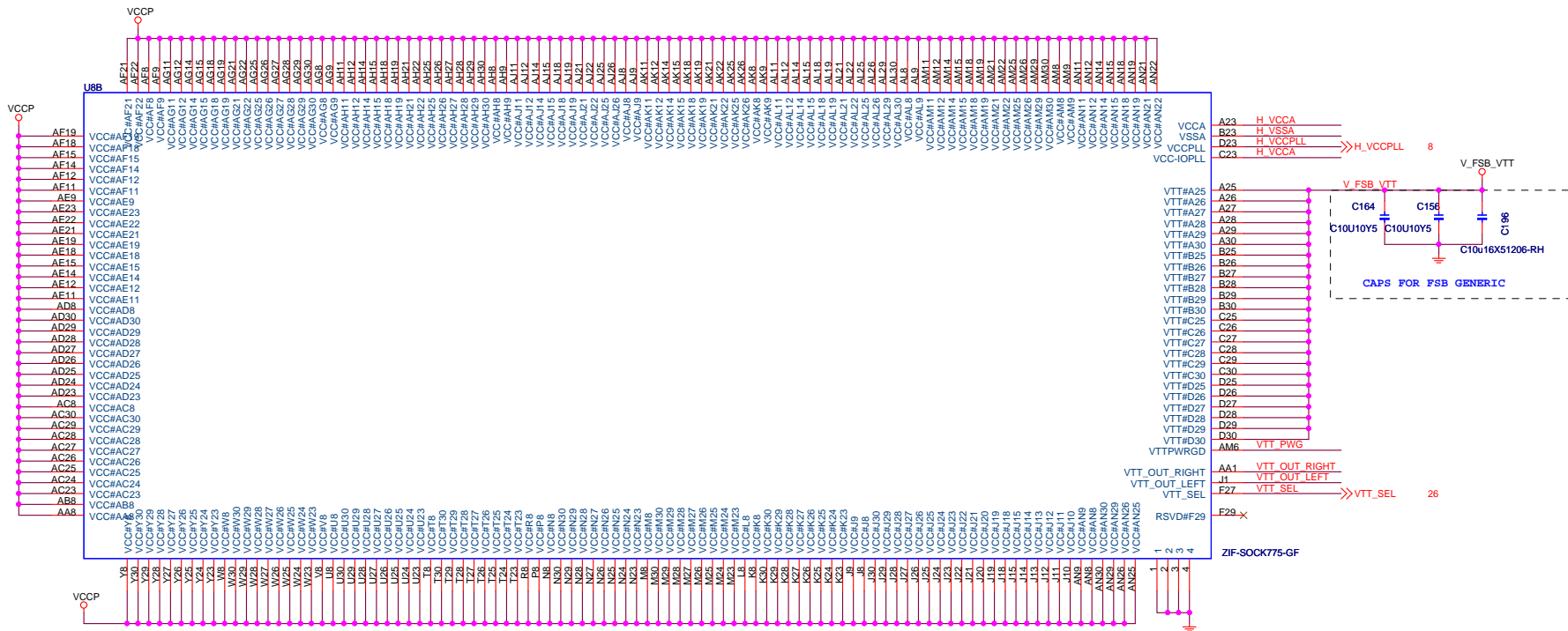


Board Stack-up

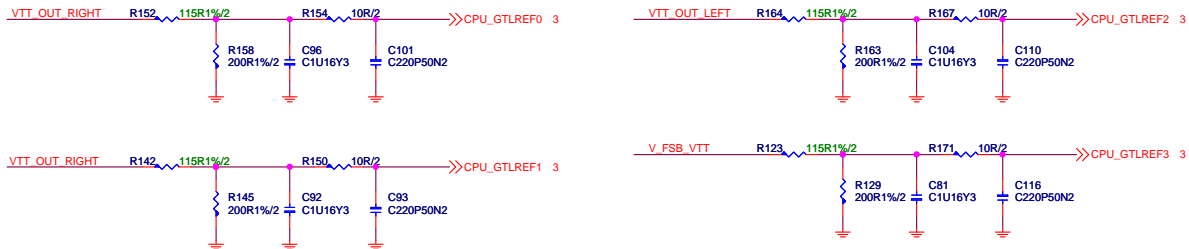
(1080 Prepreg Considerations)

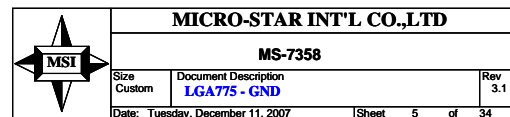


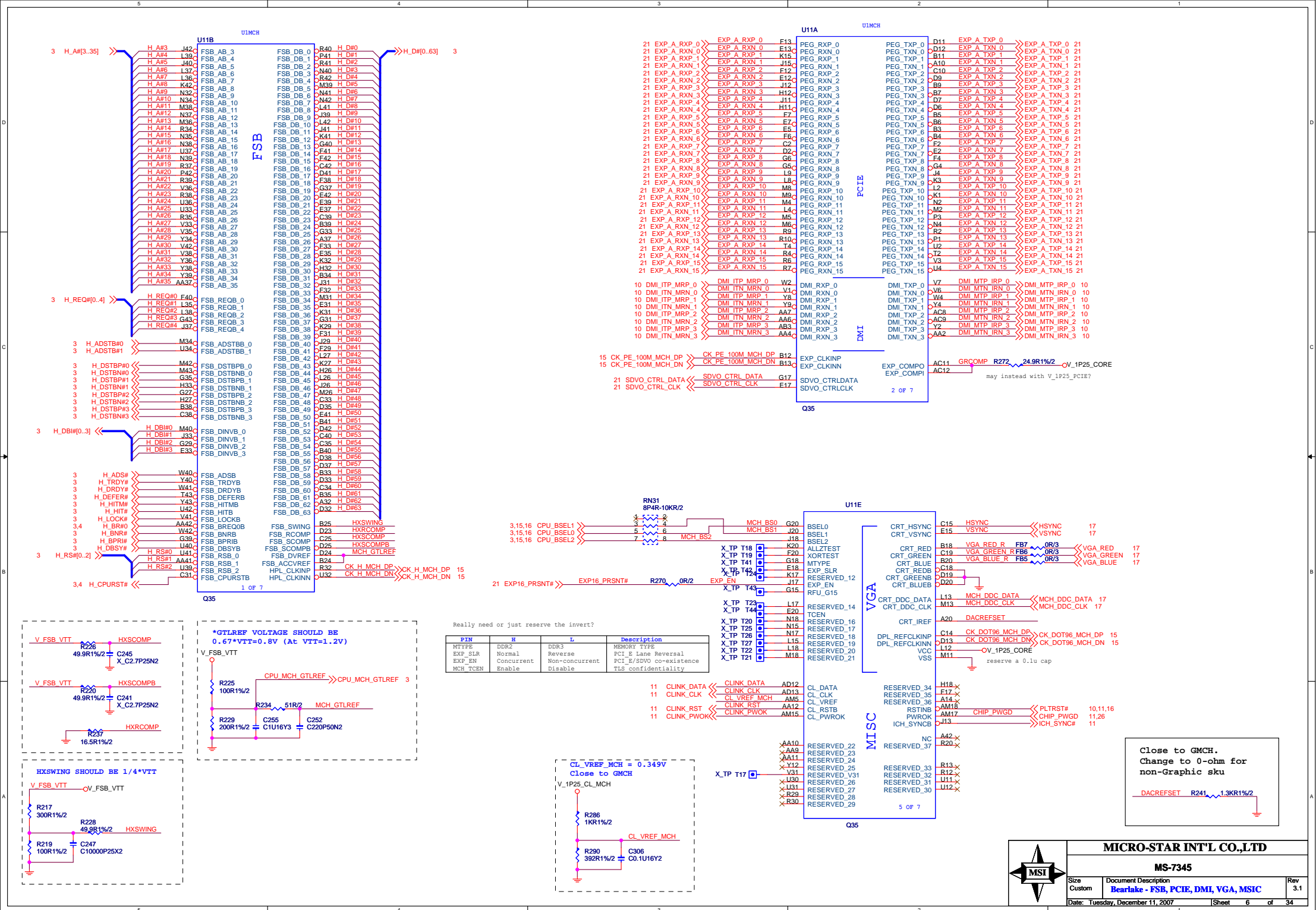
Single End 50ohm Top/Bottom : 4mils
 USB2.0 - 90ohm : 15/4.5/7.5/4.5/15
 SATA - 95ohm : 15/4/8/4/15
 LAN - 100ohm : 15/4/8/4/15
 PCIE - 95ohm : 15/4/8/4/15
 IEEE1394 - 110ohm : 15/4/9/4/15
 IDE : 15/4/8/4/15

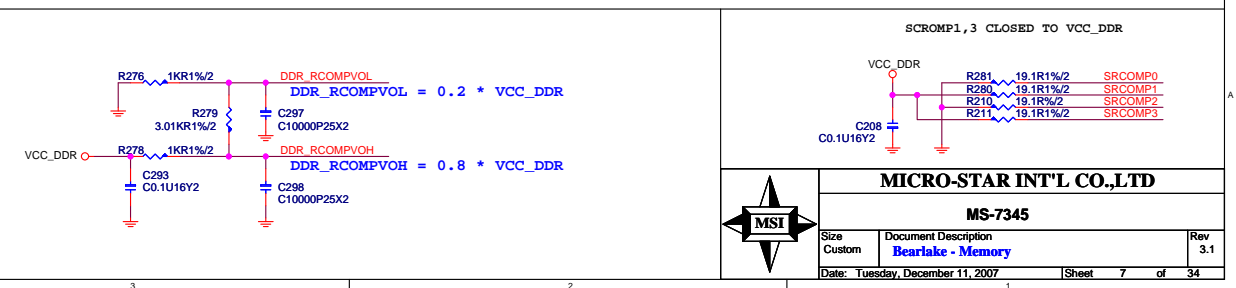
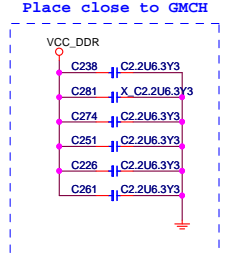
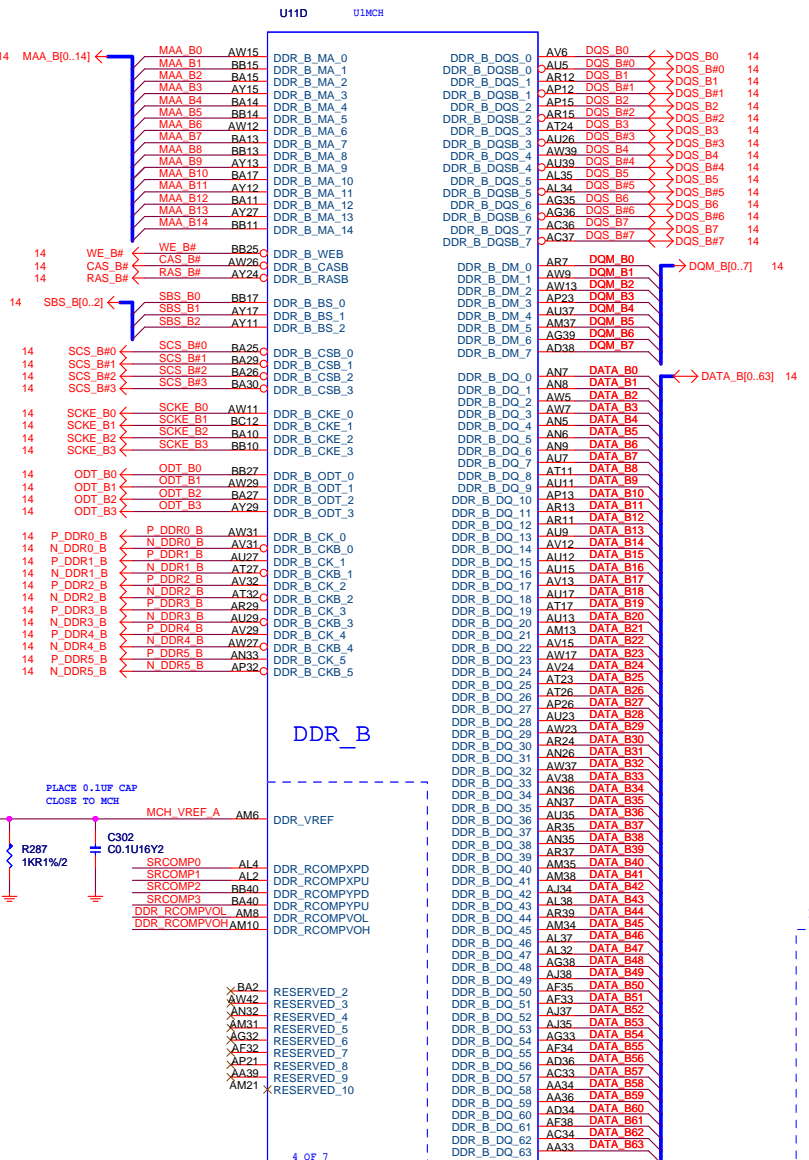
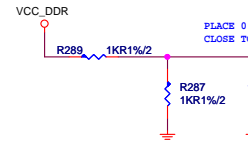
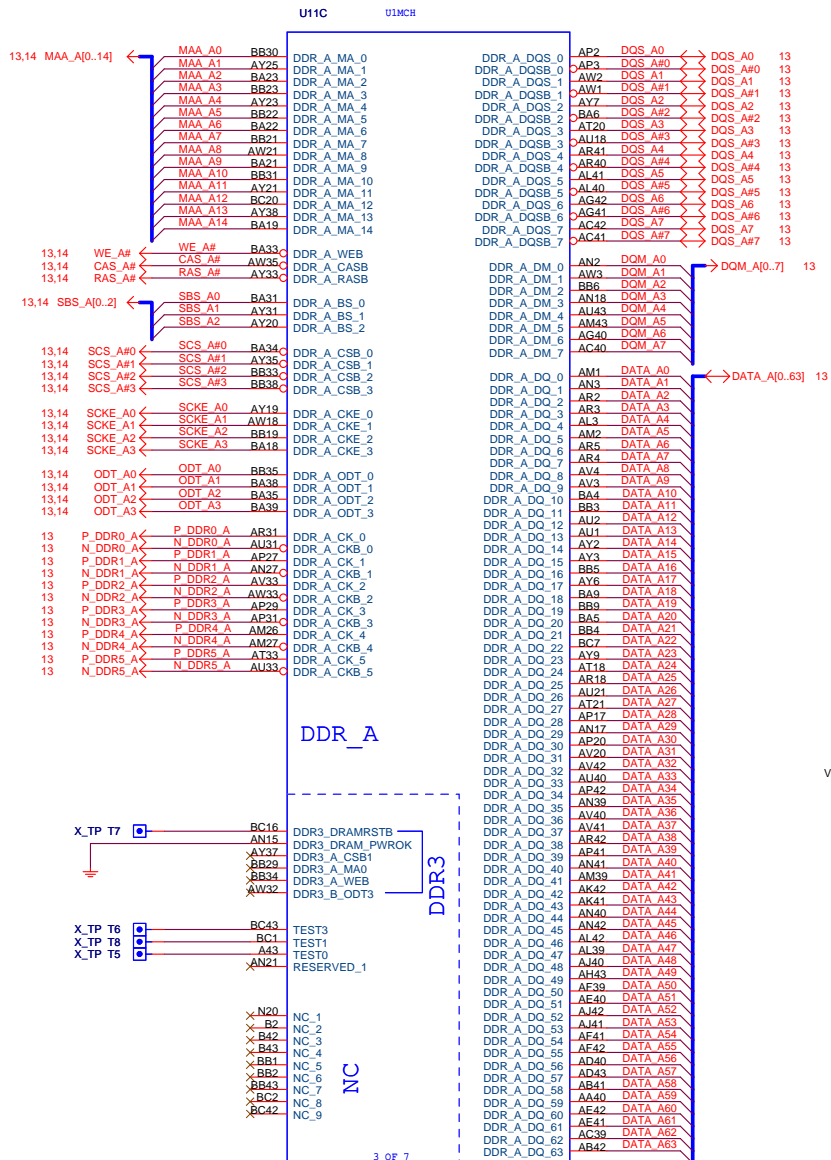


*GTLREF VOLTAGE SHOULD BE
0.67 * VTT = 0.8V (At VTT=1.2V)

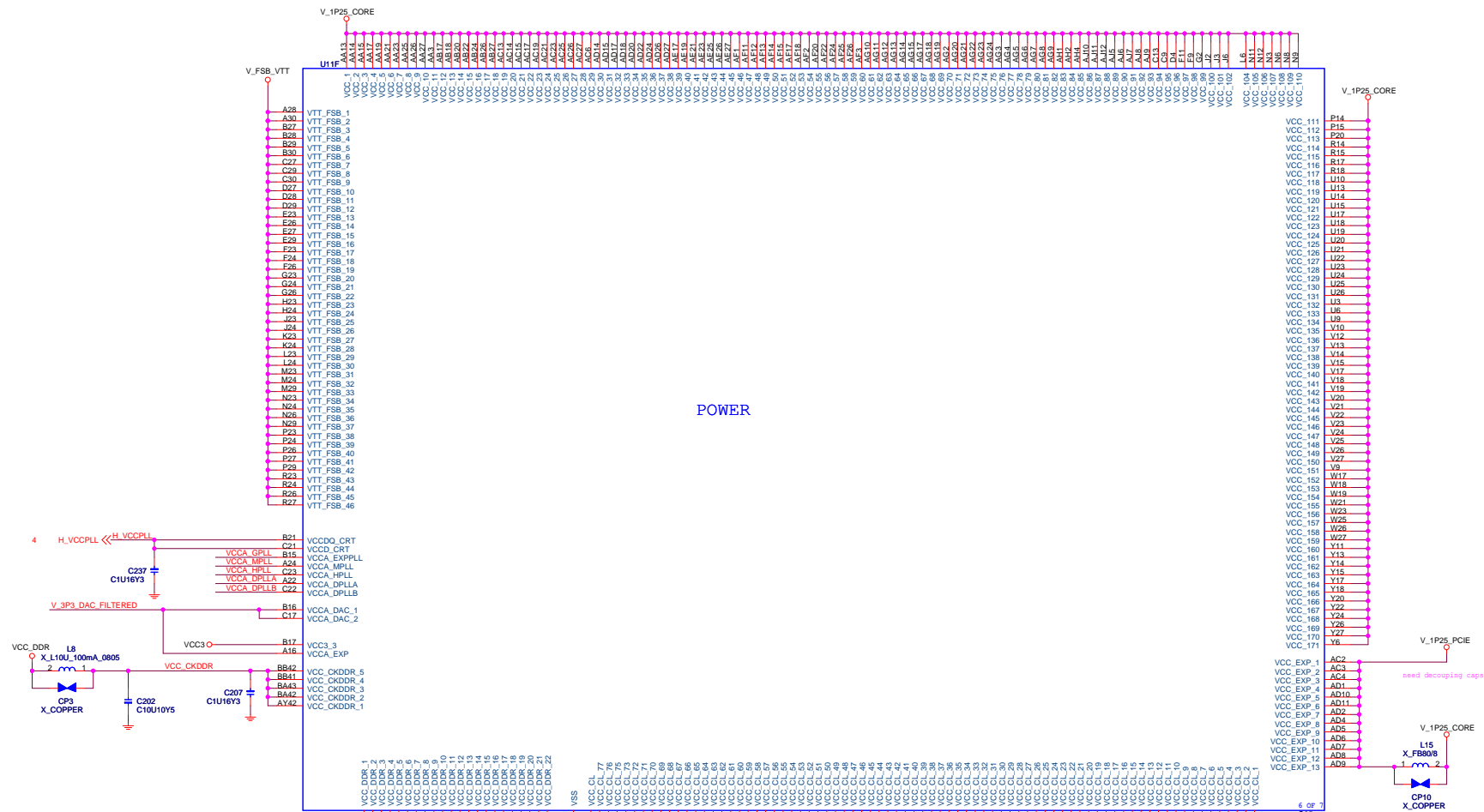
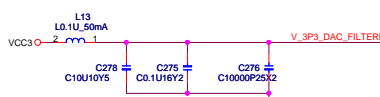
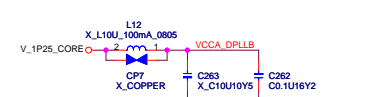
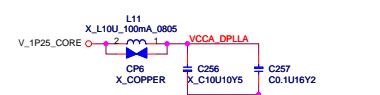
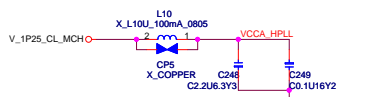
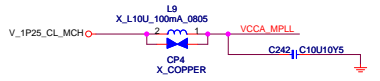
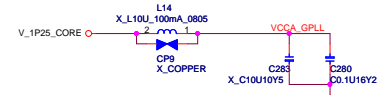


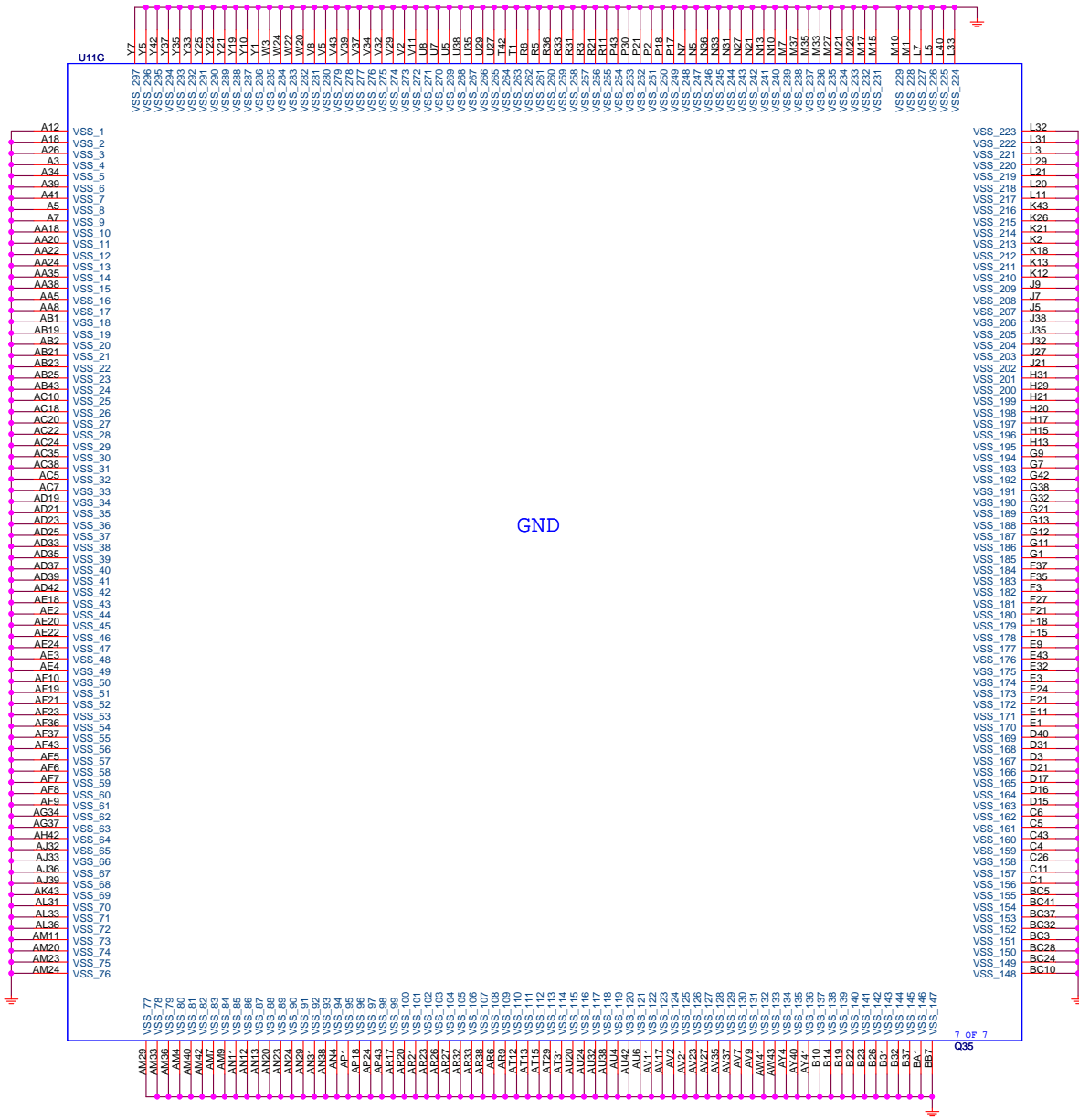


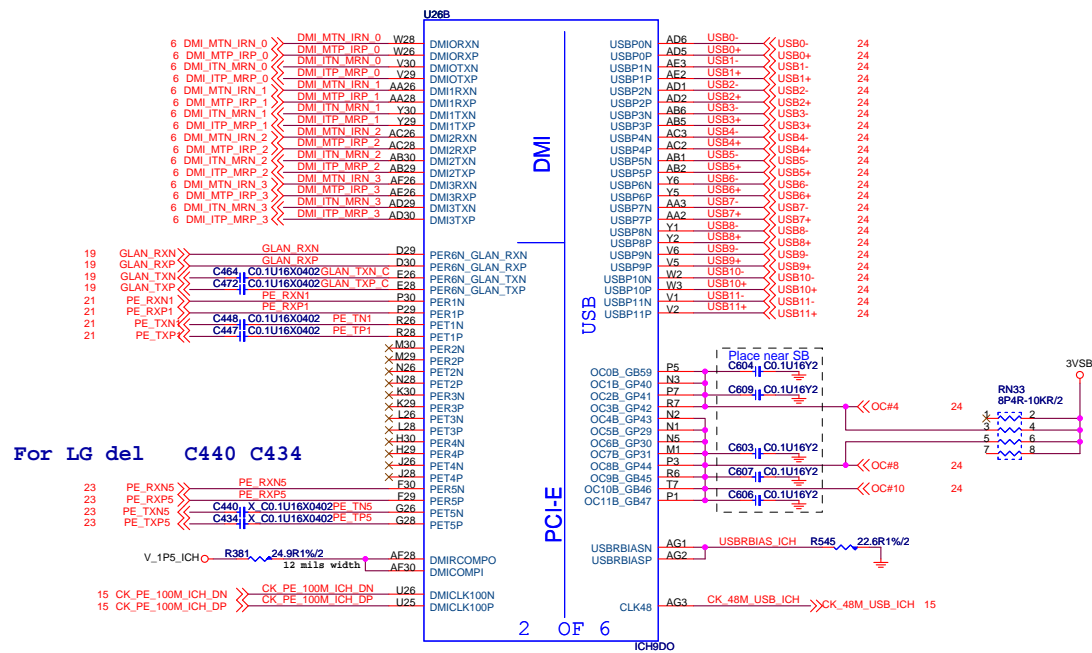




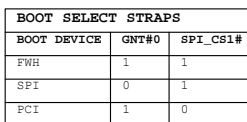
NB POWER



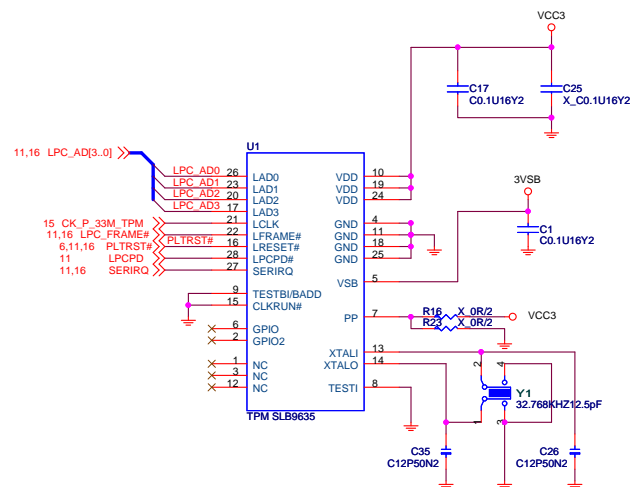


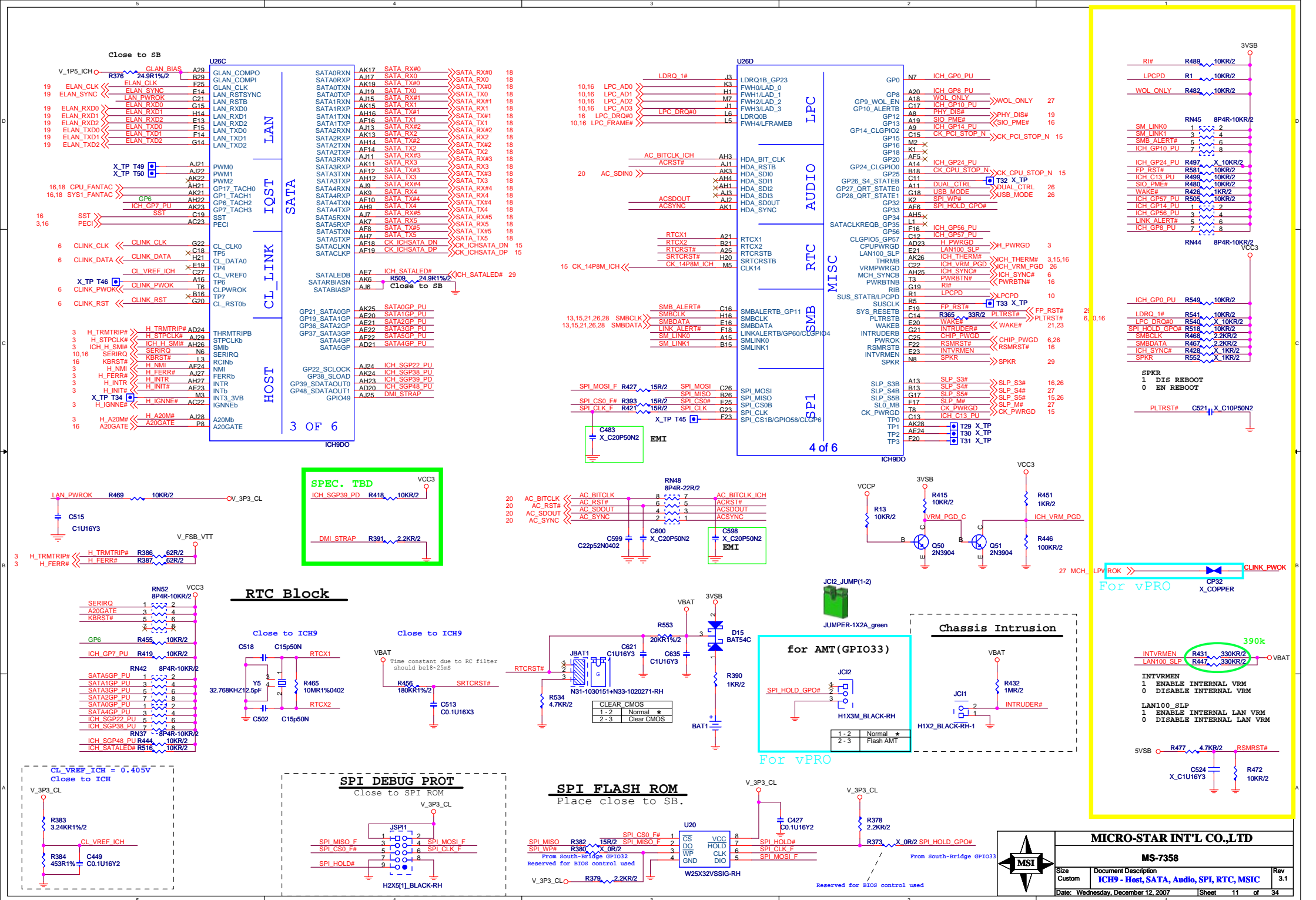


TPM - Security Controller



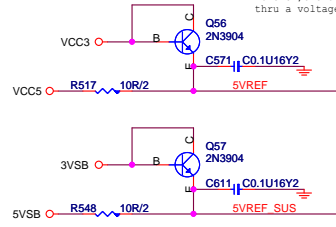
```
HDA_SDOUT/HDA_SYNC strap PCI_E port
configuration bit[1:0].Internal weak pull down.
00:1X/1X/1X/1X          11:0X/0X/4X
```



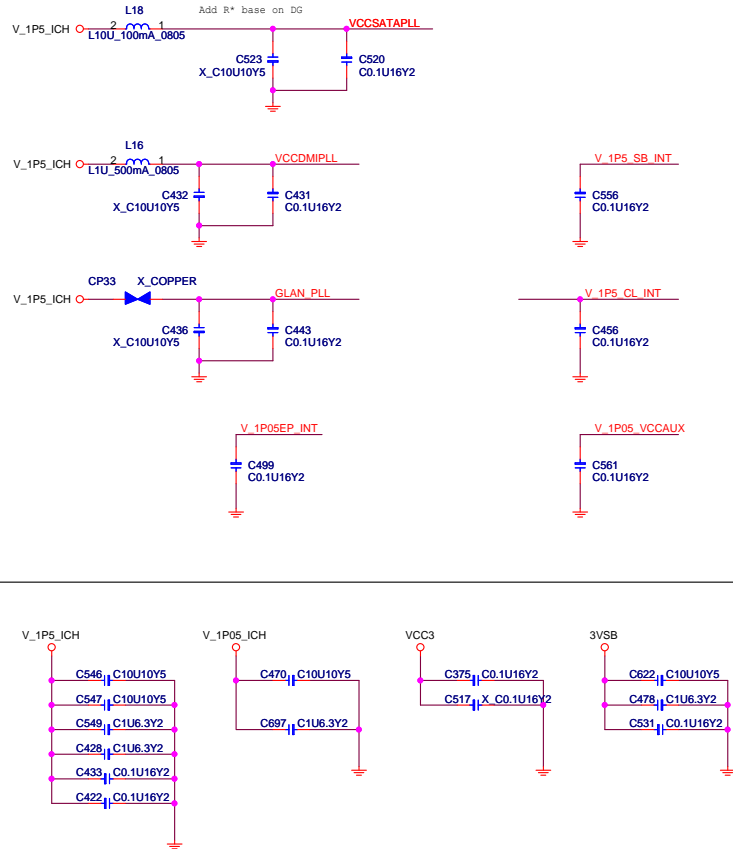


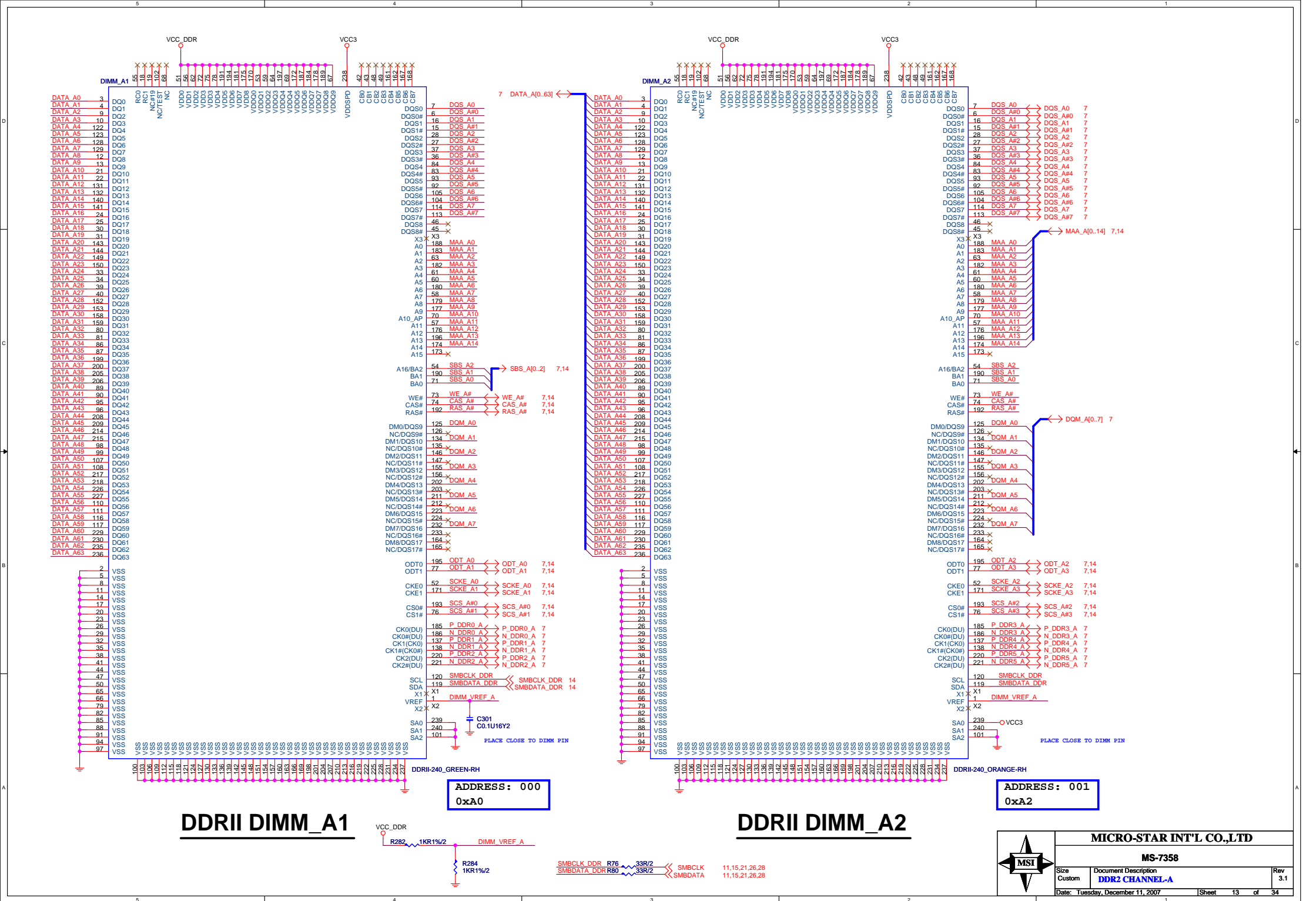
5VREF & 5VREF_SUS Sequencing Circuit

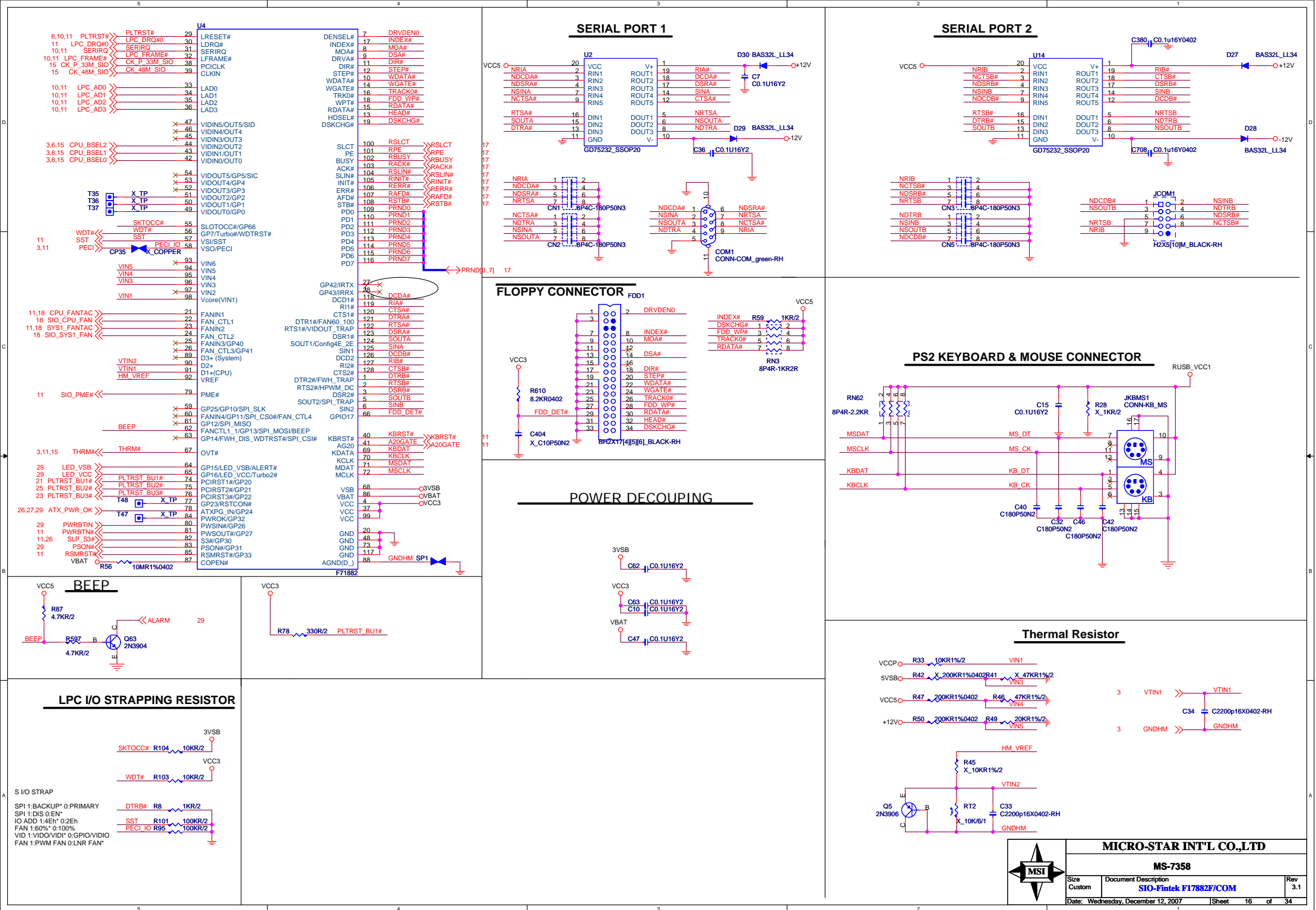
V5REF must be powered up before VCC3 or after VCC3 within 0.7V.
Also, V5REF must power down after VCC3 or before VCC3 within 0.7V.
This rule is also applies to V5REF_SUS and 3VSB.
However, the 3VSB is derived from the 5VSB on the power supply thru a voltage regulator and therefore, they can satisfy the requirement.



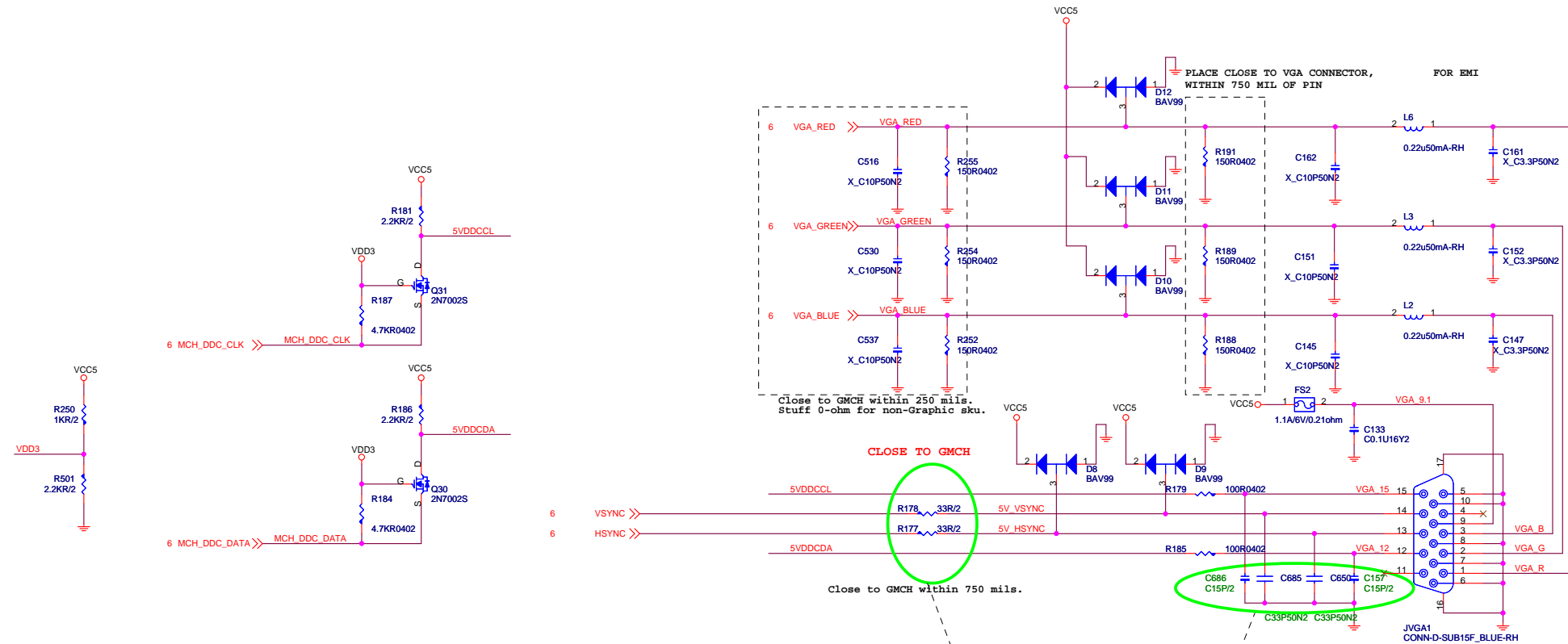
SB POWER



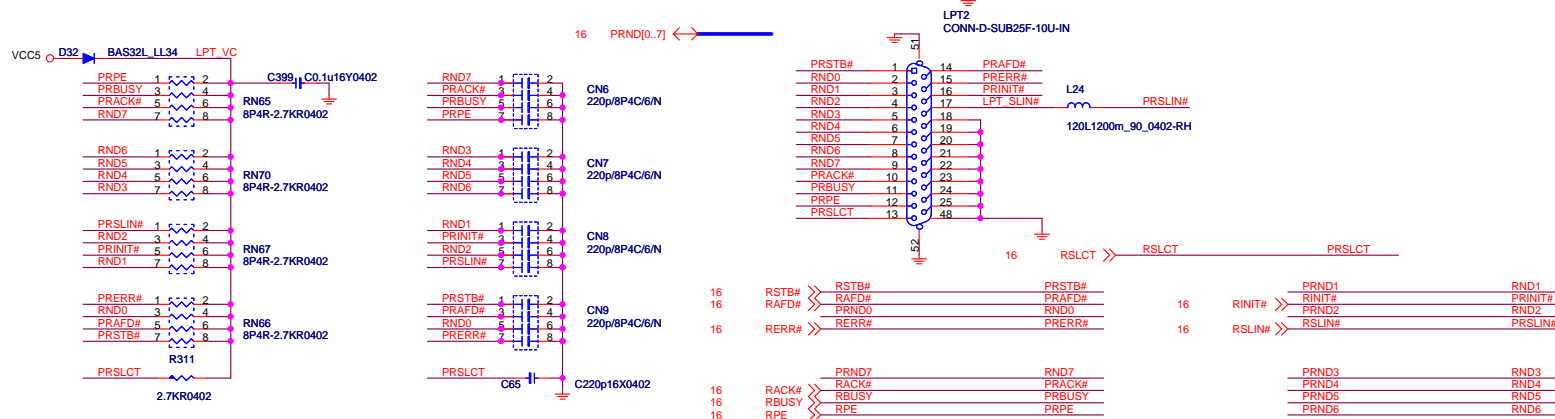




Video Connector



PARALLAL PORT

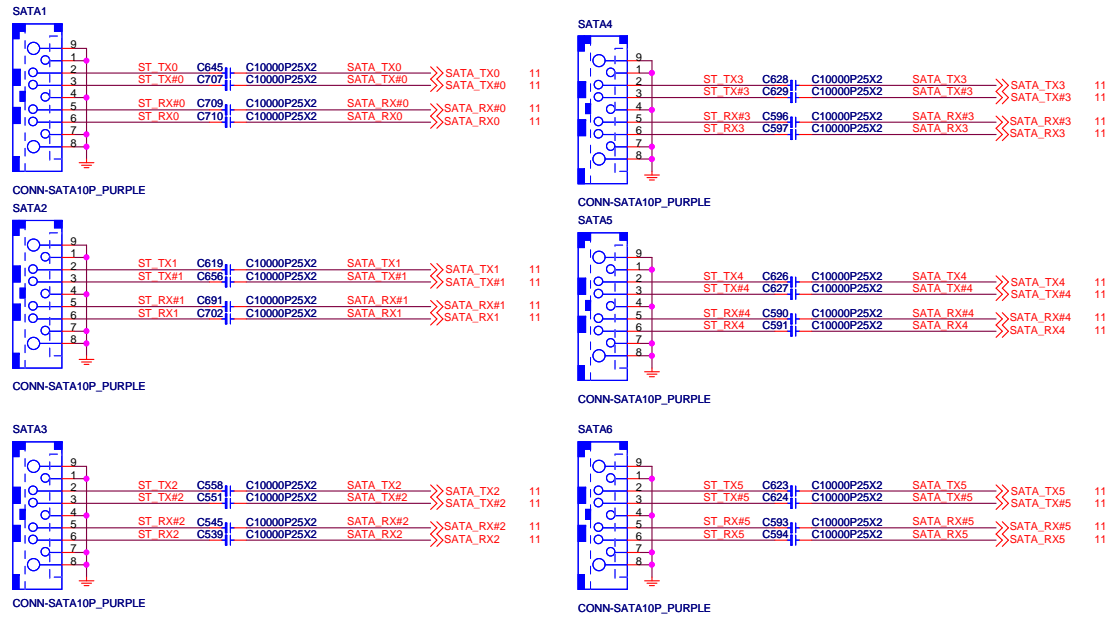


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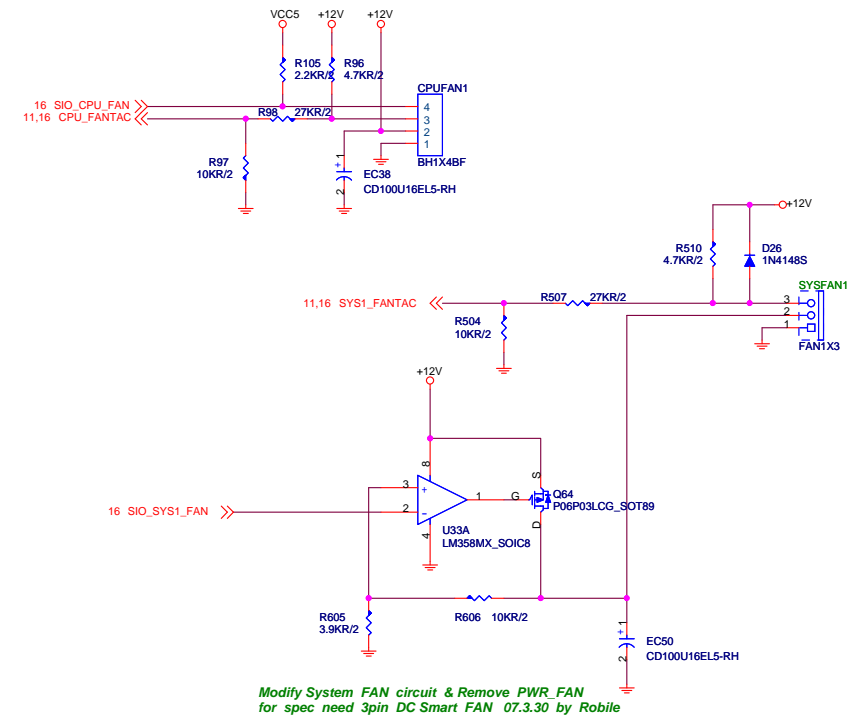
Size Custom	Document Description VGA	Rev 3.1
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SATA 1- 6 PORT



james modify

FAN-COUNTROL CIRCUIT

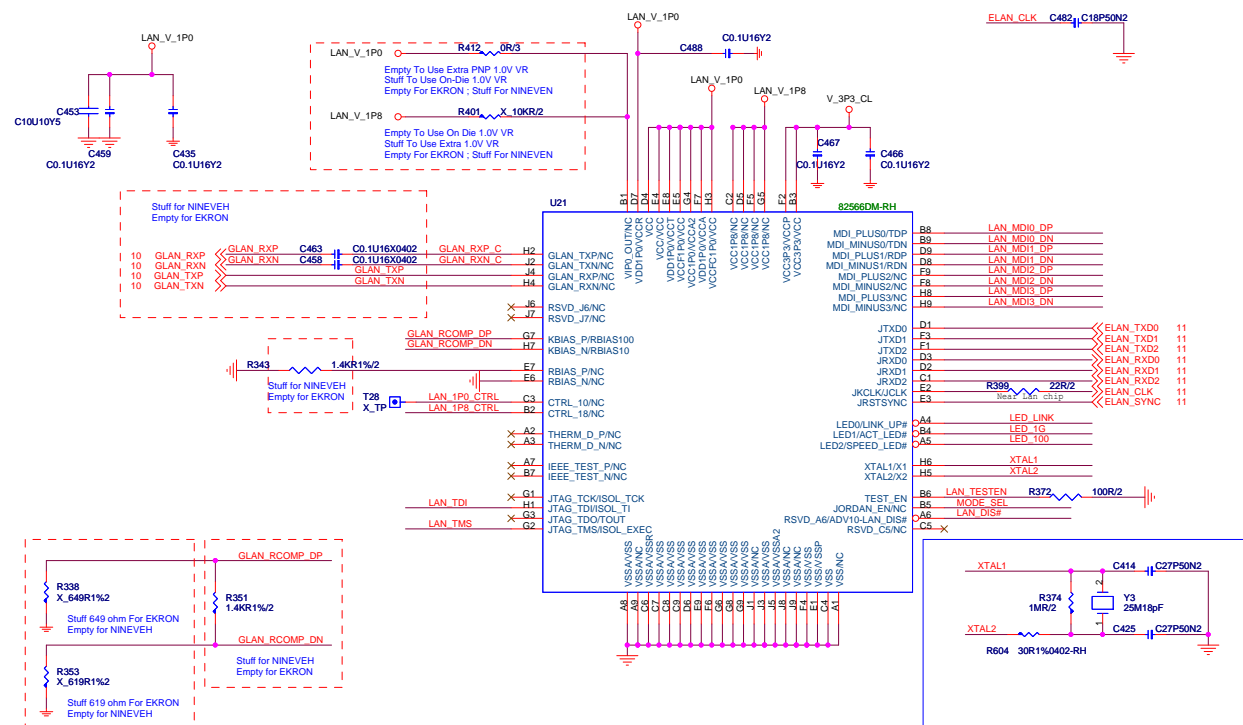


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LAN - NINEVEH/EKRON



B06-8256605-1Y6
FOR NECP CONSIGN,CHIP LAN,INTEL®82566DM,,BGA-81pin,NINEVEH GIGA LAN CHIP(PHY),RoHS COMPLIANCE
Intel 82566DM
 For business desktop PCs.Support Intel AMT2 or ASF 2.0 alerting,Circuit Breaker,WoL,PXE,Multipoort teaming,RSS,Intel Stable Image Platform Program drivers.
Intel 82566DM
 For consumer desktop PC.Support Digital Home capabilities,WoL,PXE.
Intel 82562V
 Basic 10/100 Ethernet connection.

B06-8256615-K06
,CHIP LAN,INTEL®82566DC,,BGA-81pin,NINEVEH GIGA LAN CHIP(PHY),RoHS COMPLIANCE





B06-8256205-K06
,CHIP LAN,INTEL®82562V,,BGA-81pin,NINEVEH GIGA LAN CHIP(PHY),RoHS COMPLIANCE

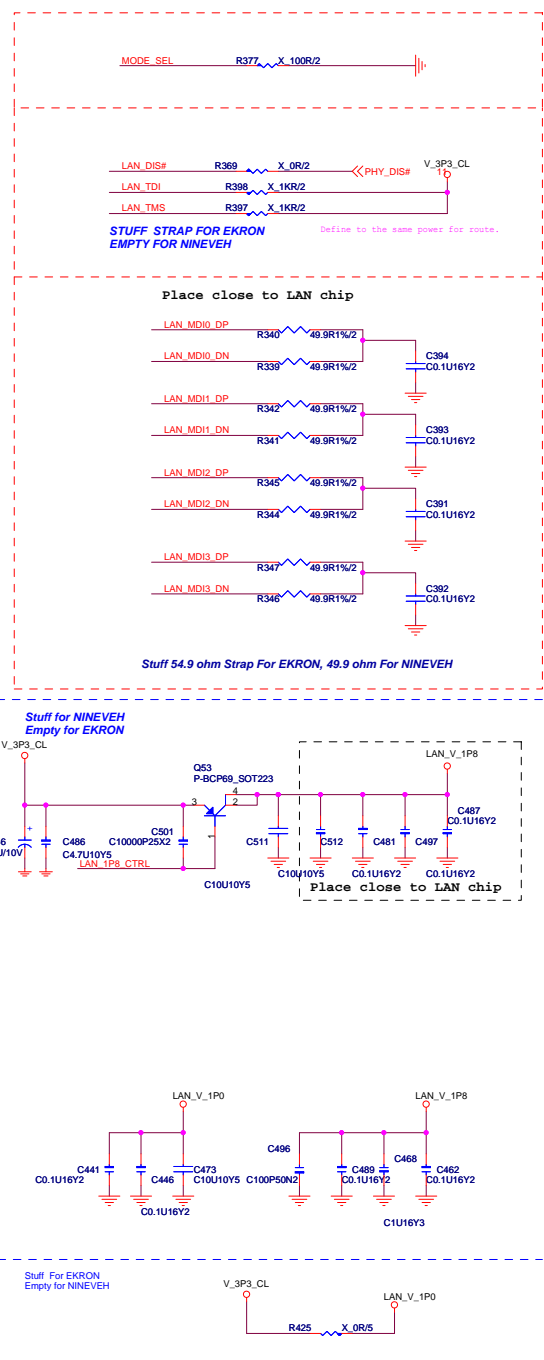
Modify Lan CLK circuit only BOM changes 07.3.30 by Robile

```
Speed LED Type
1000Mbps : Orange
100Mbps  : Green
10Mbps   : LED off
```

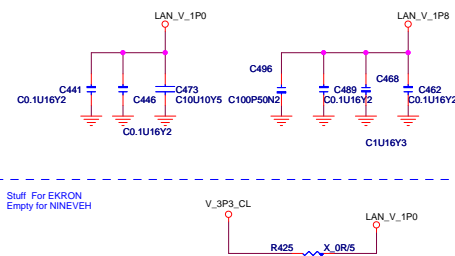
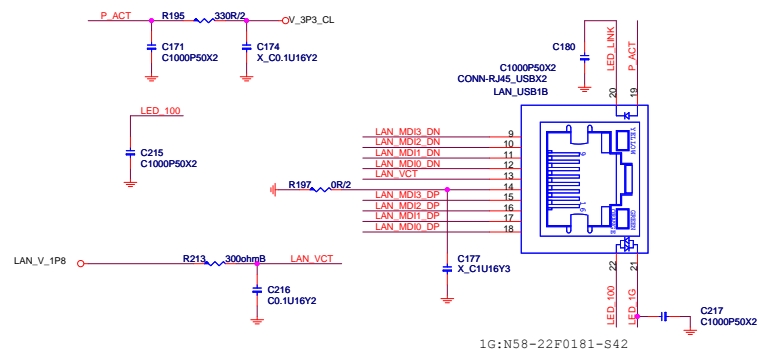
YELLOW : For Active/Link

ACT_LED	Link_LED
S0: LOW	S0: LOW
S1/S3/S4/S5: HIGH	S5: HIGH
	S1/S3/S4: WOL EN-->LOW WOL DIS-->HIGH

Giga-Lan		10/100-Lan	
N56-22F0181-642		N58-22F0061-64 N58-22F0011-F0	
Link	Yellow	Link	Yellow
Active	Blinking	Active	Blinking
1000	Orange	100	Green
100	Green	10	None
10	None		
19		19	
20	Yellow	20	Yellow
21	Orange	21	
			
22	Green	22	Green



LAN CONNECTOR

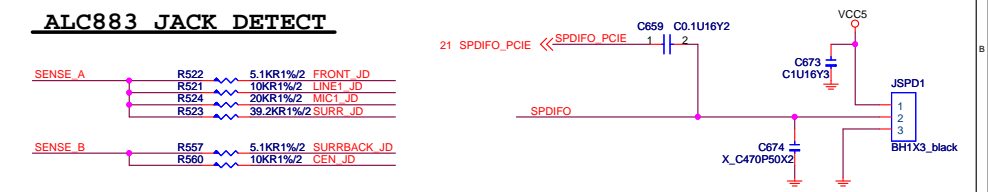
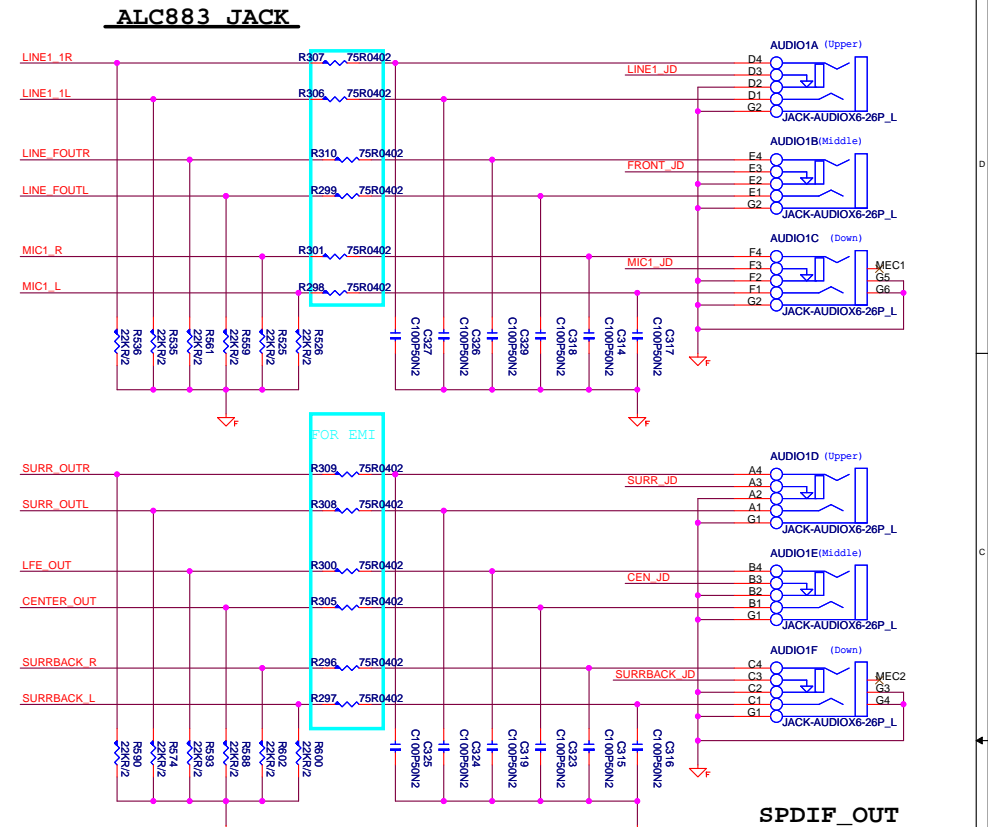
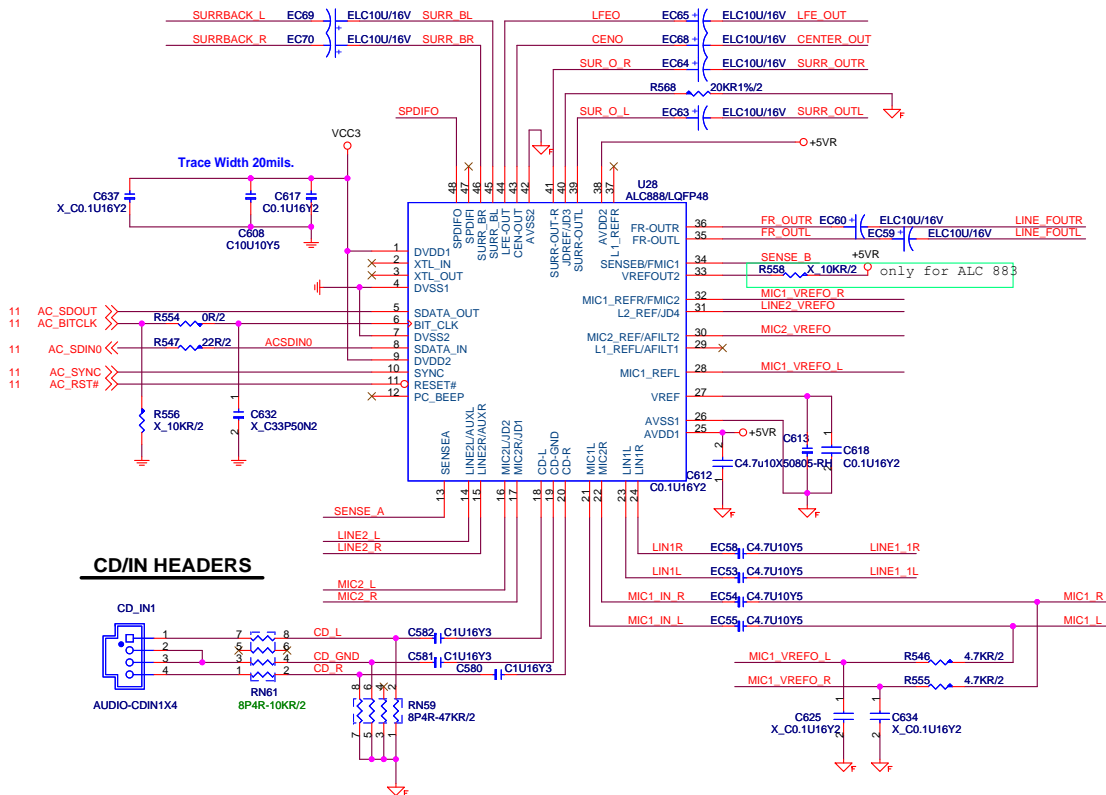


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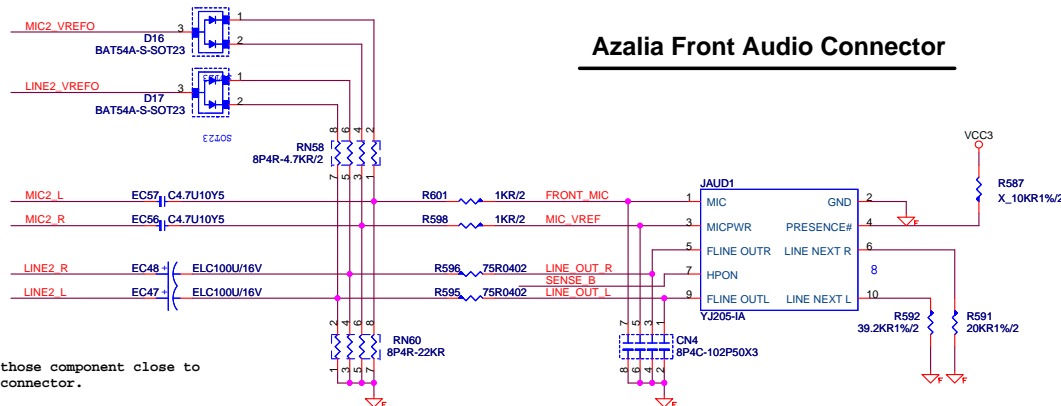
MS-7358

Size Custom	Document Description LAN NINEVEH/EKRON	Re
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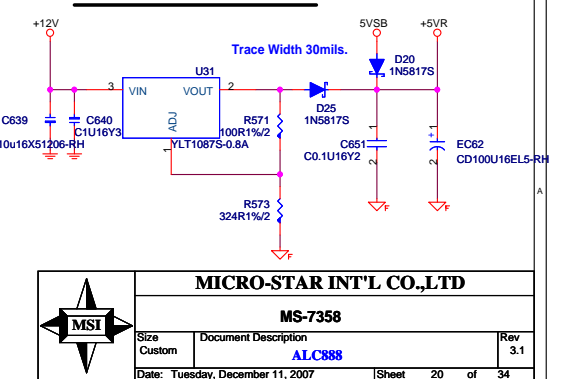
ALC888 CODEC



Azalia Front Audio Connector

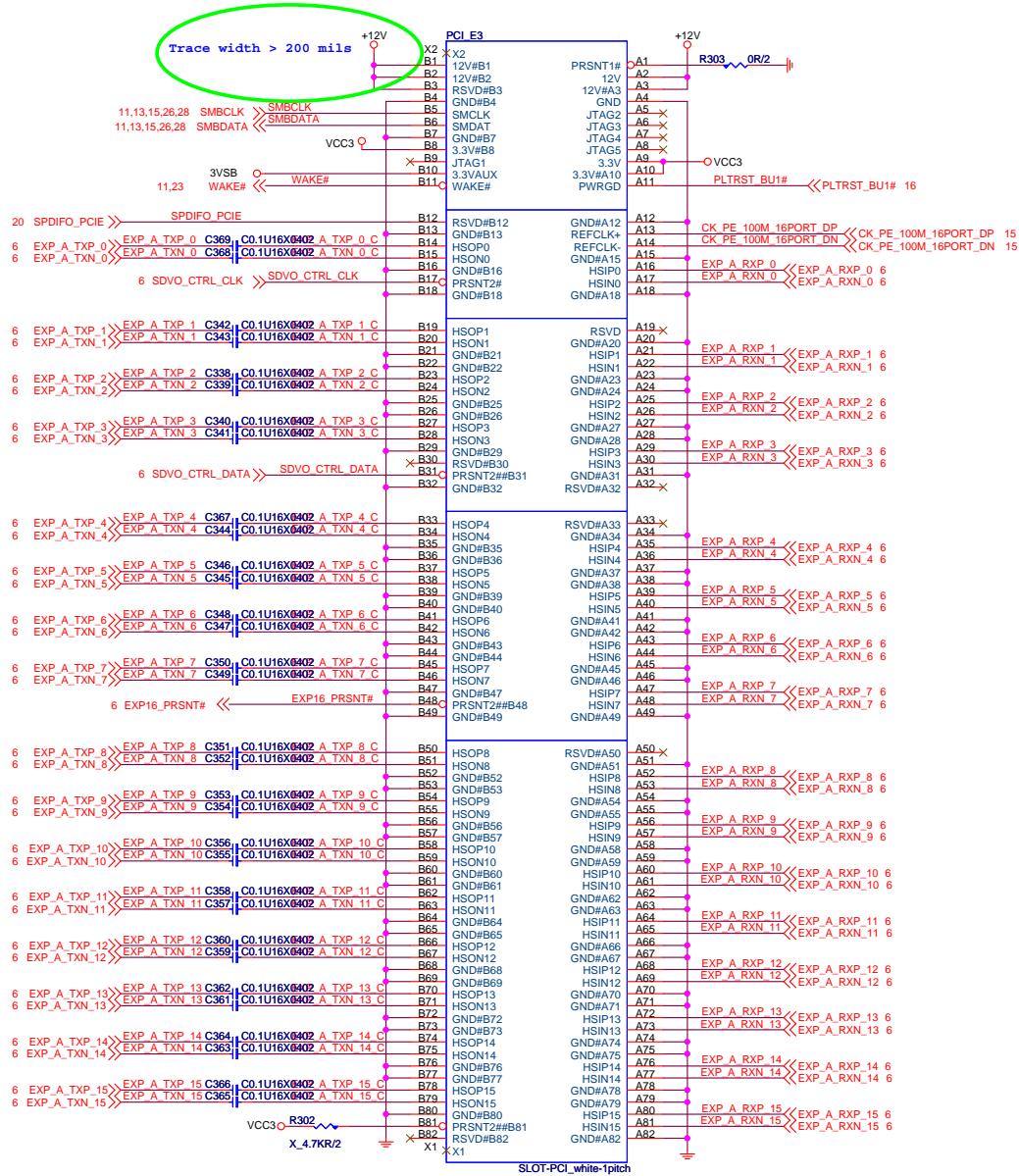


AUDIO CODE REGULATORS

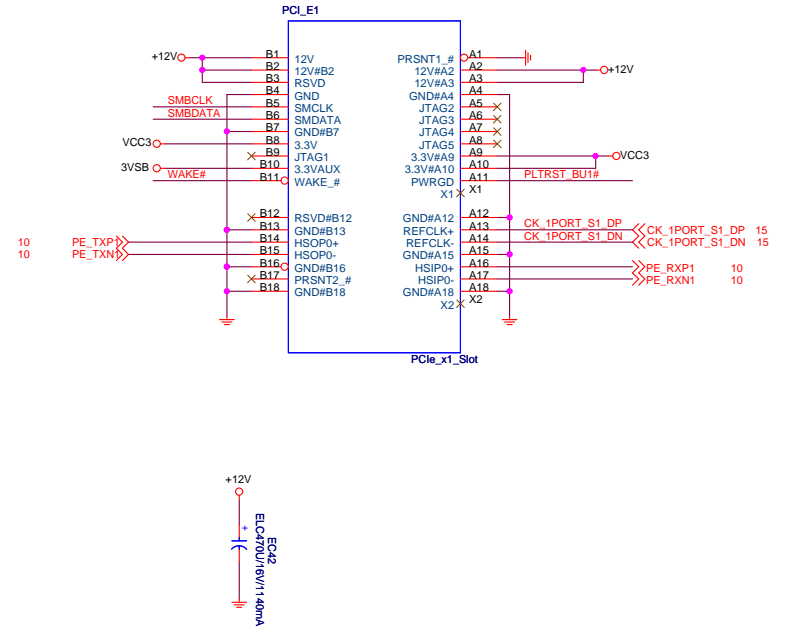


Place those component close to audio connector.

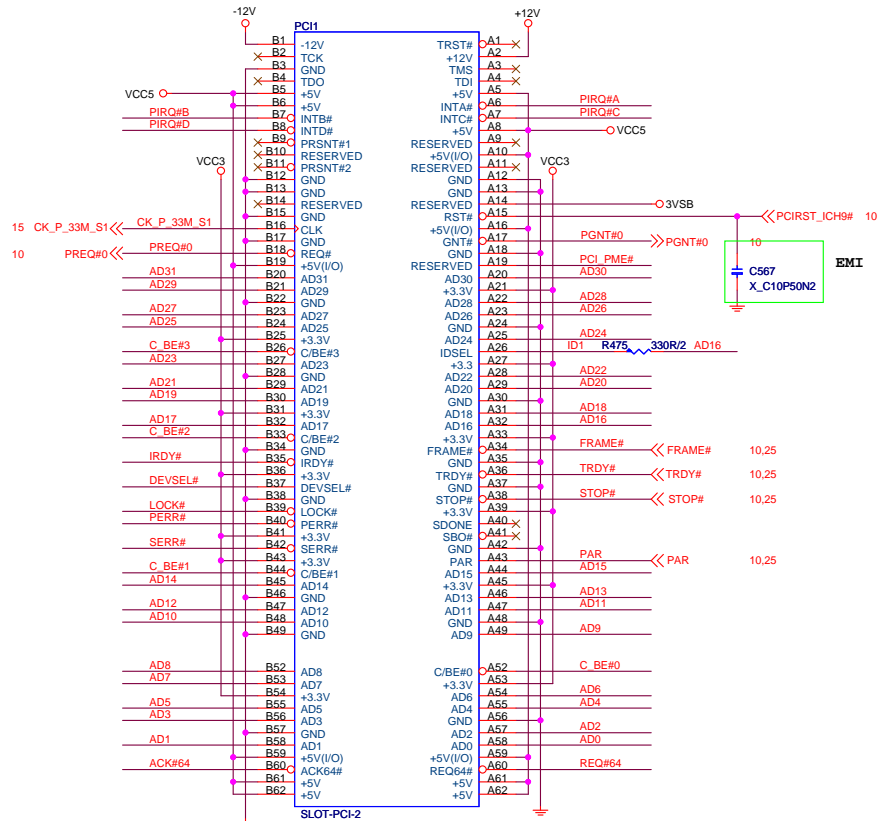
PCI_Express X16 Slot



PCI_Express X4 Slot (Share with PCI_E x1 Slots)



PCI SLOT 1 (PCI VER: 2.2 COMPLY)



IDSEL = AD16

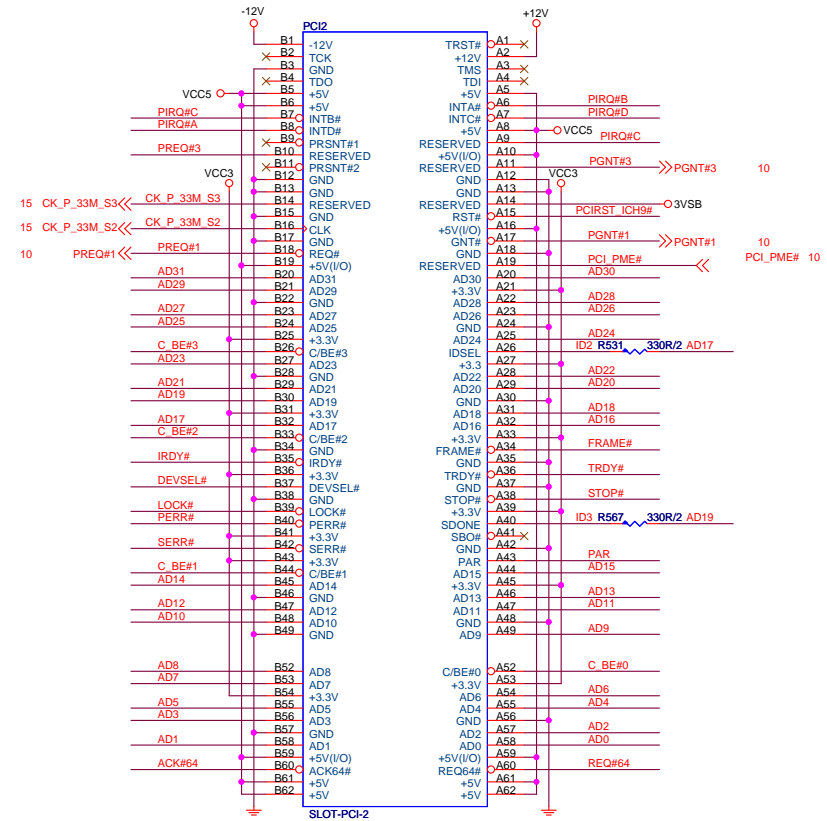
MASTER = PREQ#0

PIRQ#A

10.25 AD[31..0] << AD[31..0]

10.25 C_BE#[3..0] << C_BE#[3..0]

PCI SLOT 2 (PCI VER: 2.2 COMPLY)

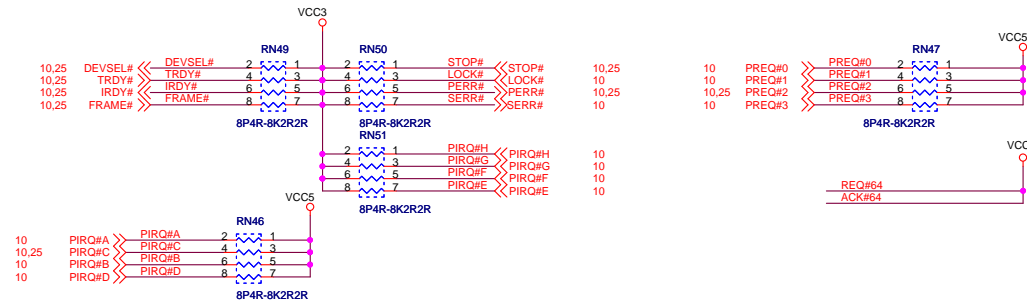


IDSEL = AD17

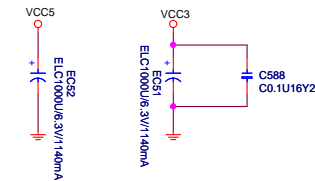
MASTER = PREQ#1

PIRQ#B

PCI PULL-UP / DOWN RESISTORS



PCI SLOT DECOUPLING CAPACITORS

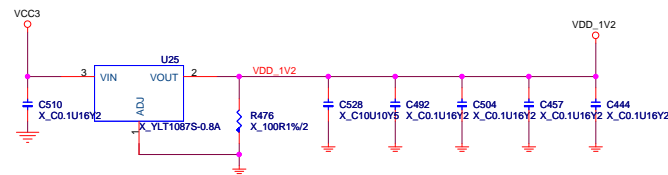
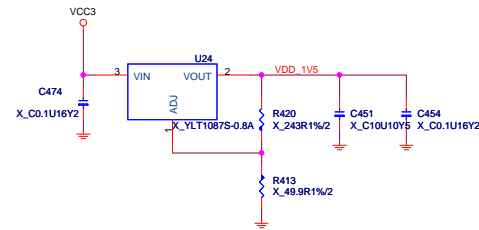
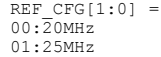


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Custom	PCI Slot 1 & 2	3.1
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```
REF_CFG[1:0] =
00:20MHz
01:25MHz
```

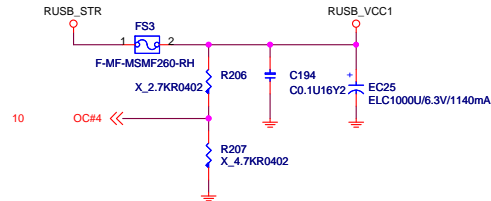
[illegible]

Size Custom	Document Description Marvell 88SE6111 PCIE to PATA/SATA	Rev 3.1
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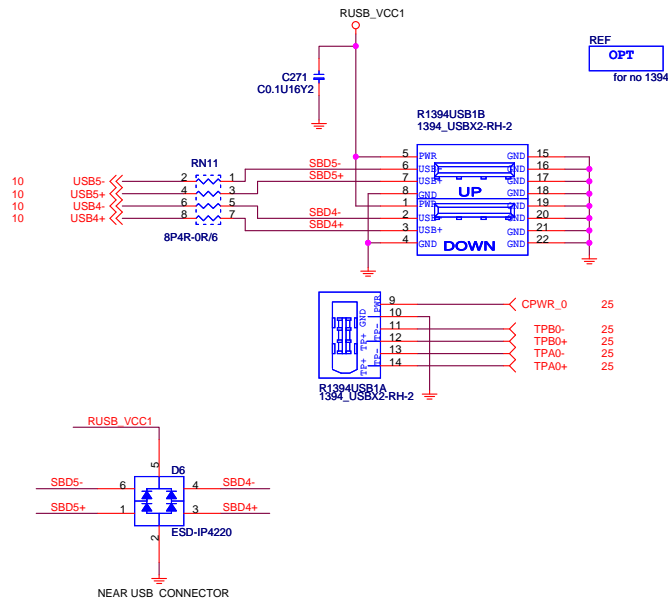
Rear USB Connector

USB POWER FOR PORT 1,2,3,4

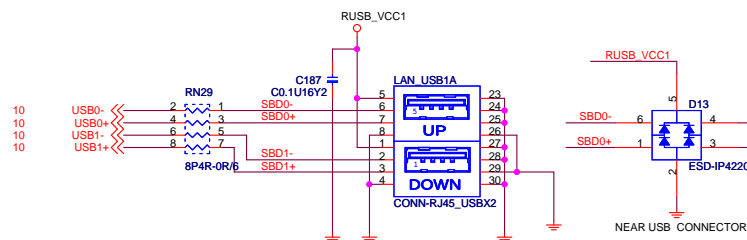
NEAR CONNECTOR



REAR USB PORT 0,1 (1394)



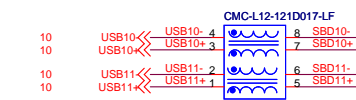
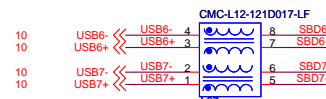
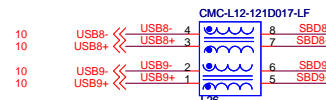
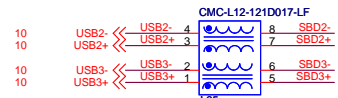
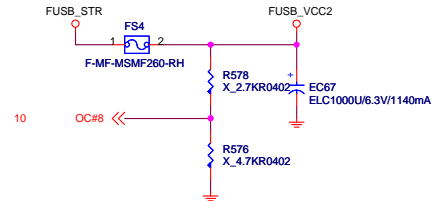
REAR USB PORT 4,5 (With LAN)



Front USB Connector

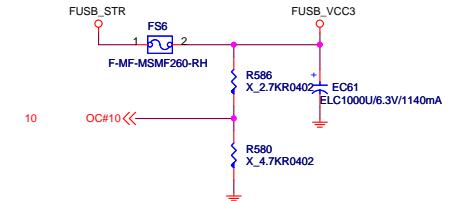
USB POWER FOR PORT 7,8,11,12

NEAR CONNECTOR

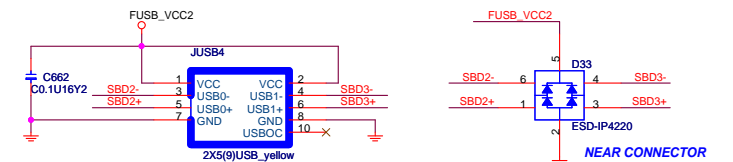


USB POWER FOR PORT 5,6,9,10

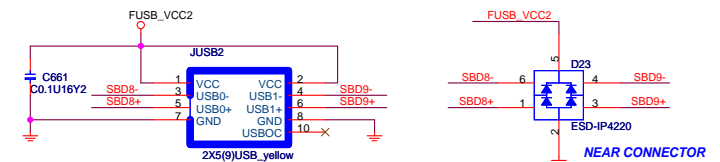
NEAR CONNECTOR



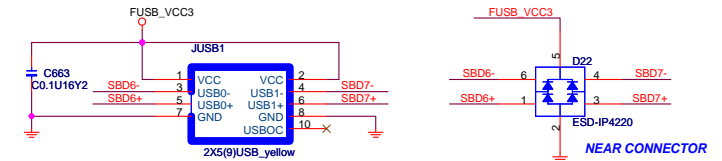
FRONT USB PORT 8,9



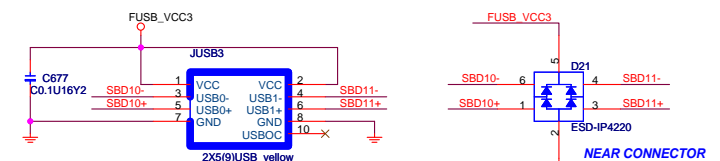
FRONT USB PORT 8,9



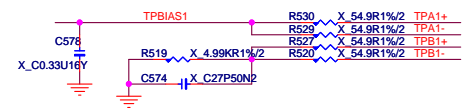
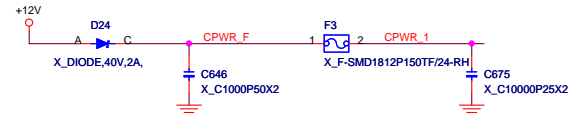
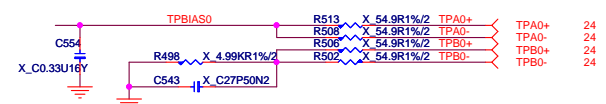
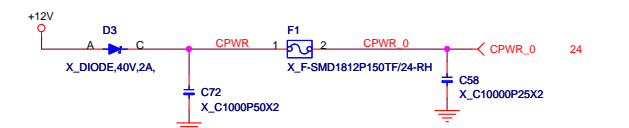
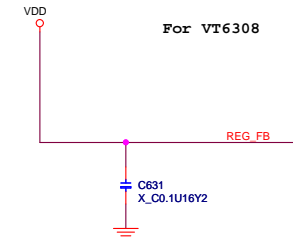
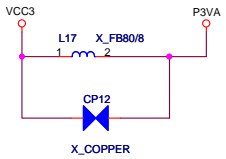
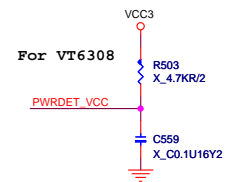
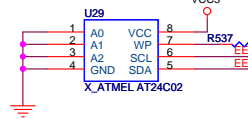
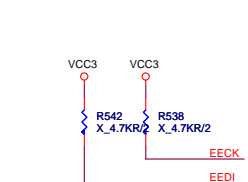
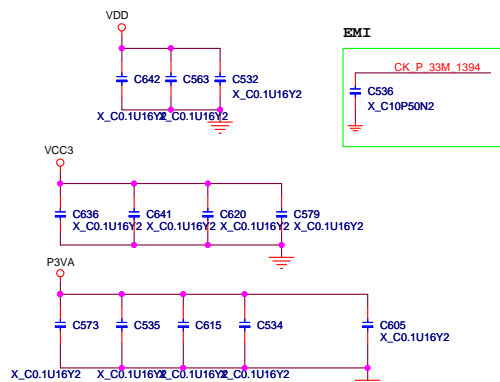
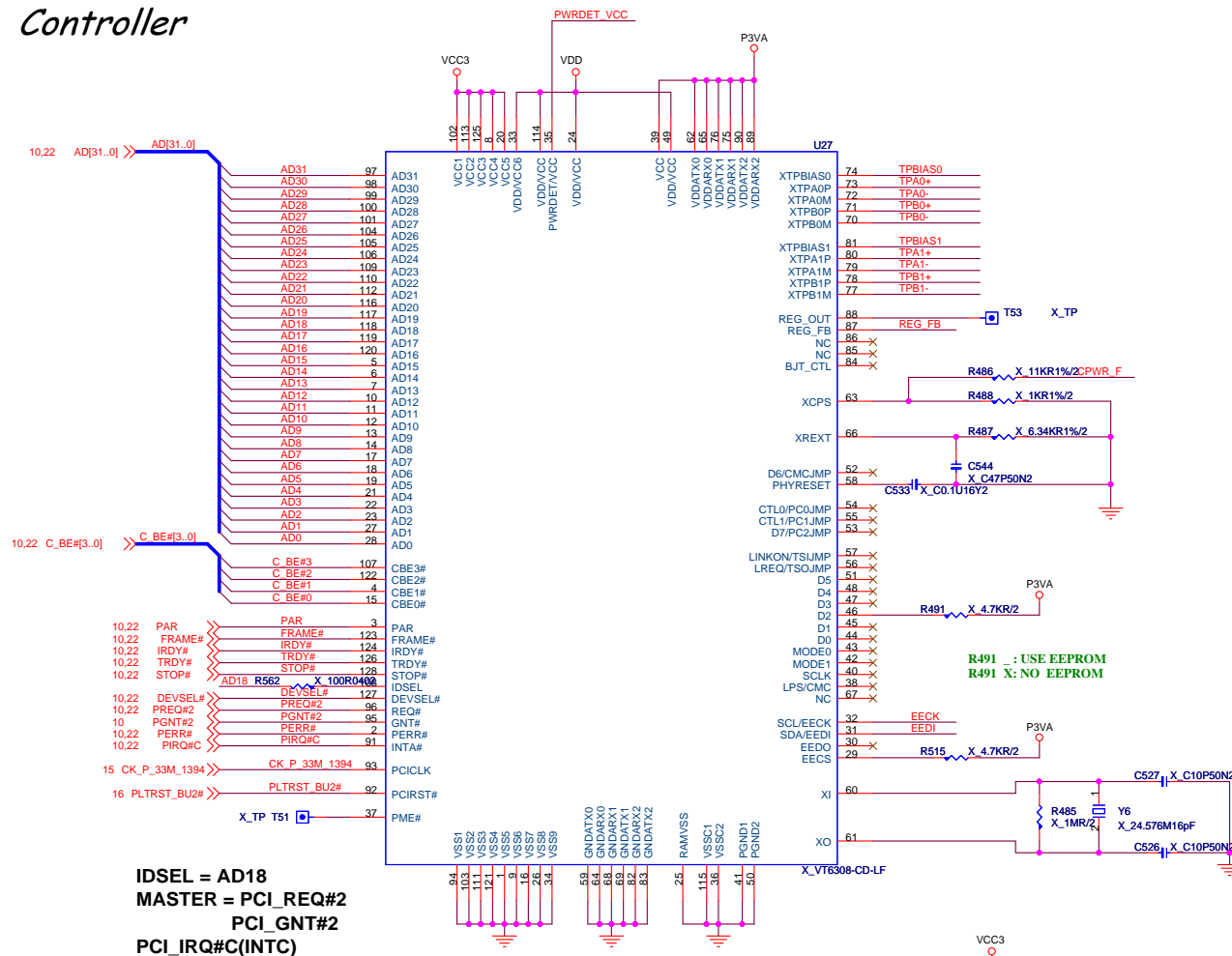
FRONT USB PORT 6,7



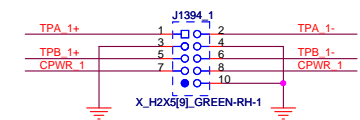
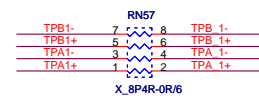
FRONT USB PORT 10,11



1394a OHCI Link Layer Controller



For LG del all



For Intel 1394 pinheader

For VT6308

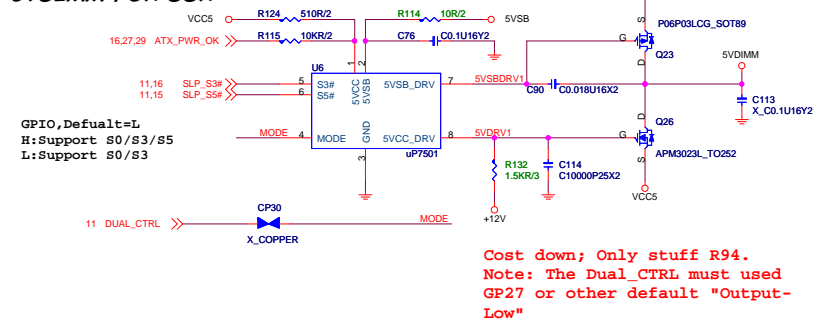


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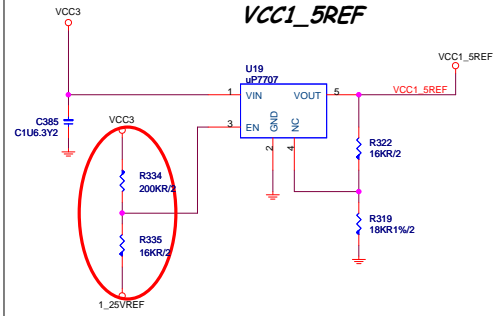
Size Custom	Document Description IEEE-1394 VIA-VT6308	Rev 3.1
Date: Wednesday, December 12, 2007	Sheet 25 of 34	

5VDIMM FOR DDR



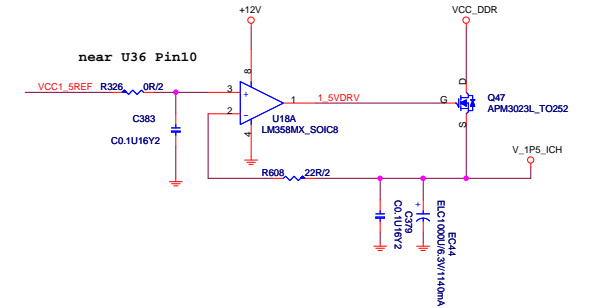
Cost down; Only stuff R94.
Note: The Dual_CTRL must used
GP27 or other default "Output-
Low"

VCC1_5REF

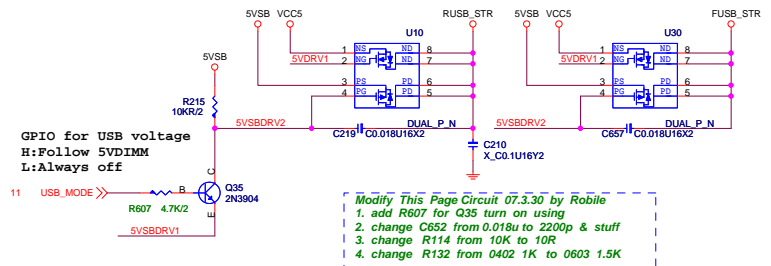


Let 1.25V and 1.5V at the same time
power up or power down

SB 1.5V 2.75A



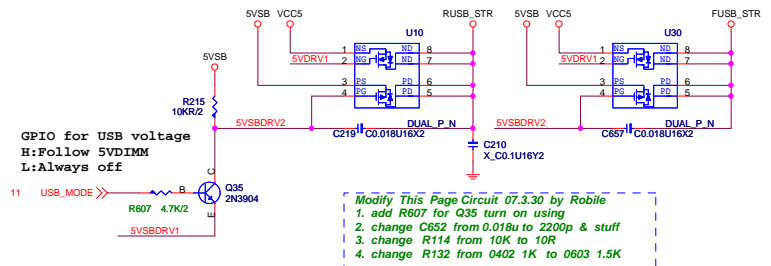
5VSB FOR Rear USB



Modify This Page Circuit 07.3.30 by Robile

1. add R607 for Q35 turn on using
2. change C652 from 0.018u to 2200p & stuff
3. change R114 from 10K to 10R
4. change R132 from 0402 1K to 0603 1.5K

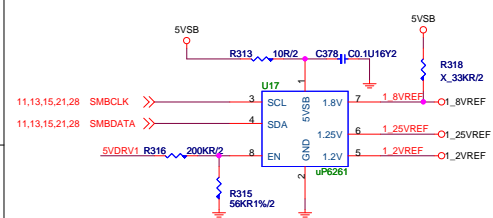
5VSB FOR Front USB



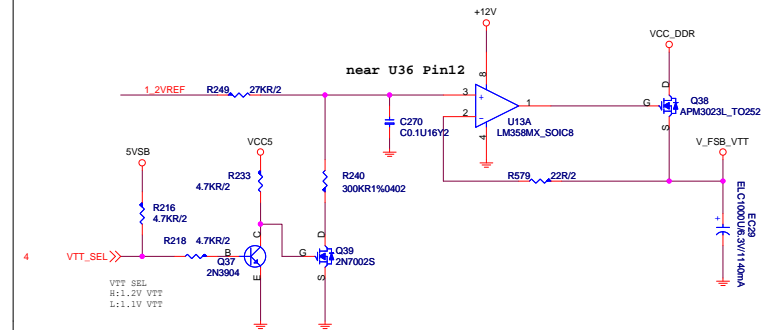
```
*Reference sinking/sourcing 100uA
*Reference ramp-up 5mS
*5VSB > 4.2V POR
*Pin8 > 1.dV Enable
*Pin8 < 0.4V Disable
```

Stuff R361 to prevent the source current not enough
issue (5.1-1.8)/33K=100uA

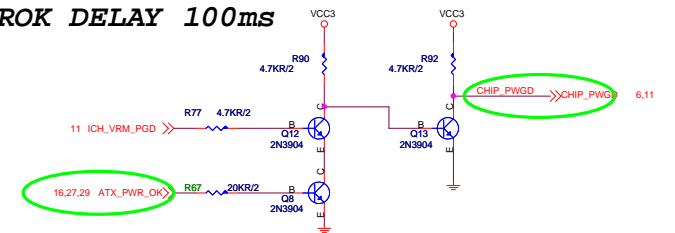
reference Voltage



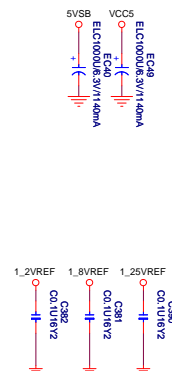
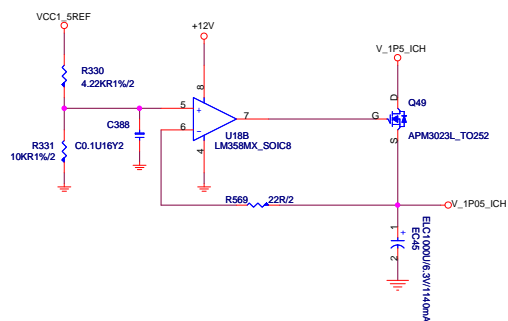
1.2V 5.8A



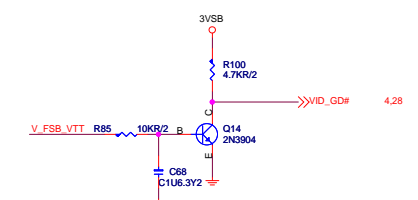
PWROK DELAY 100ms



SB 1.05V 2A

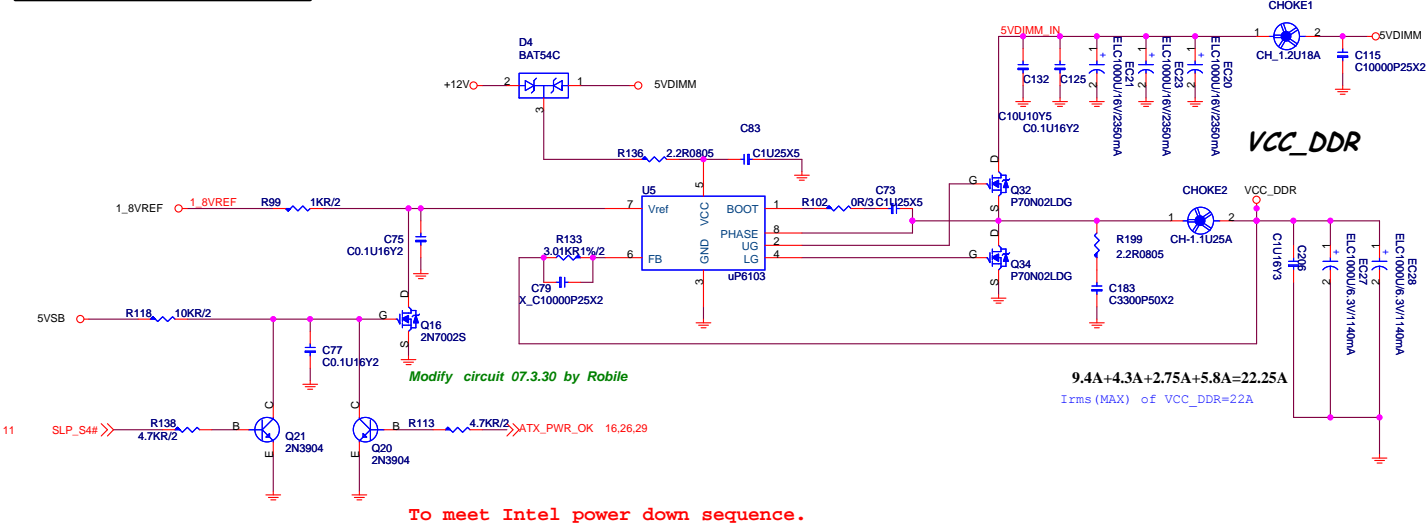


VID before PWROK >3ms

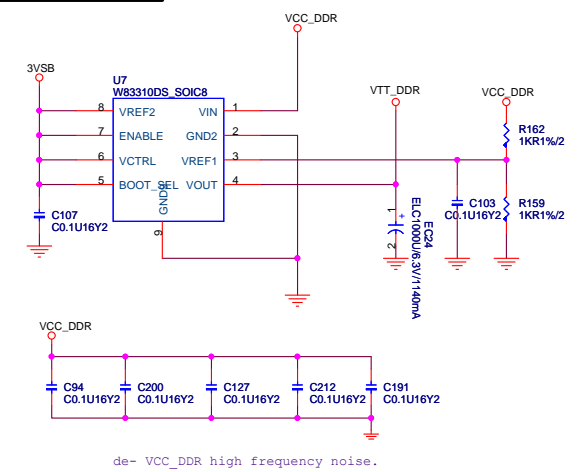


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Size Custom	Document Description ACPI controller UPI		Rev 3.1
Date: Tuesday, December 11, 2007		Sheet 26 of 34	

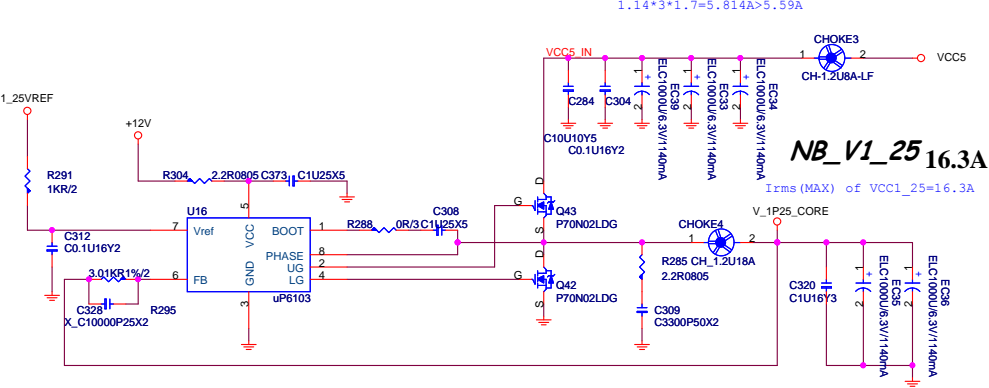
DDR II 1.8V POWER



DDR VTT Power

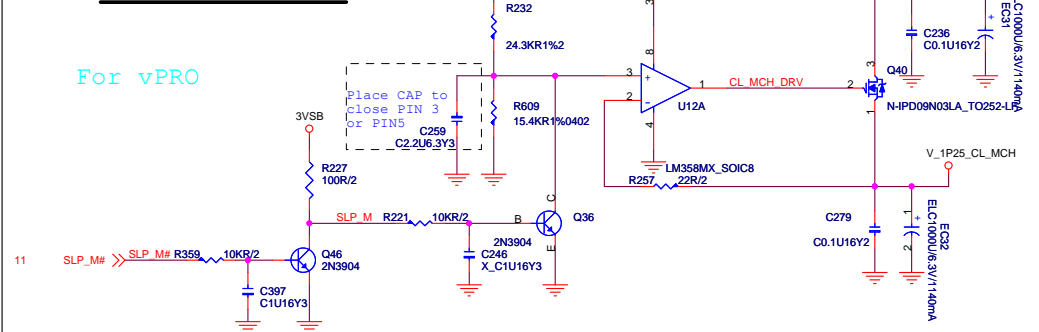


NB 1.25V POWER

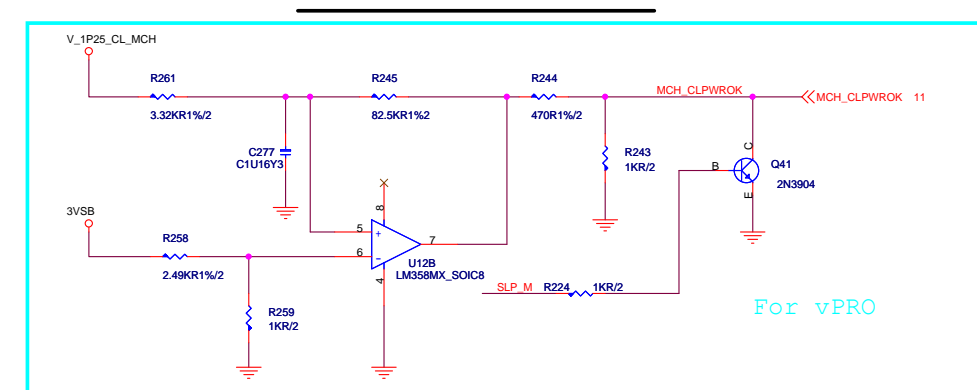


AMT POWER

V_1P25_CL_MCH (4.3A)

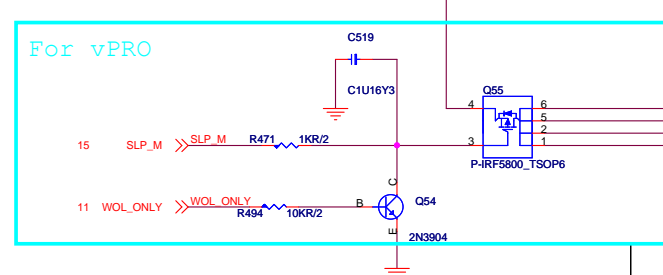


CLINK PWROK GENERATION



V_3P3_CL

(711mA)



For ViiV

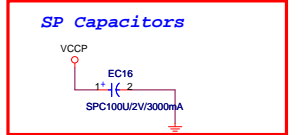
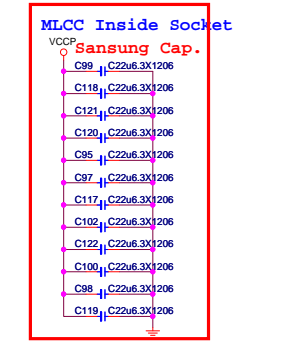
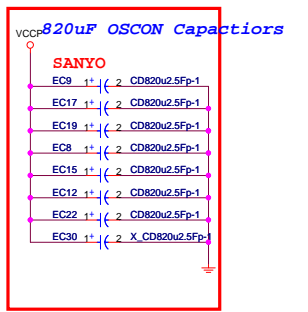
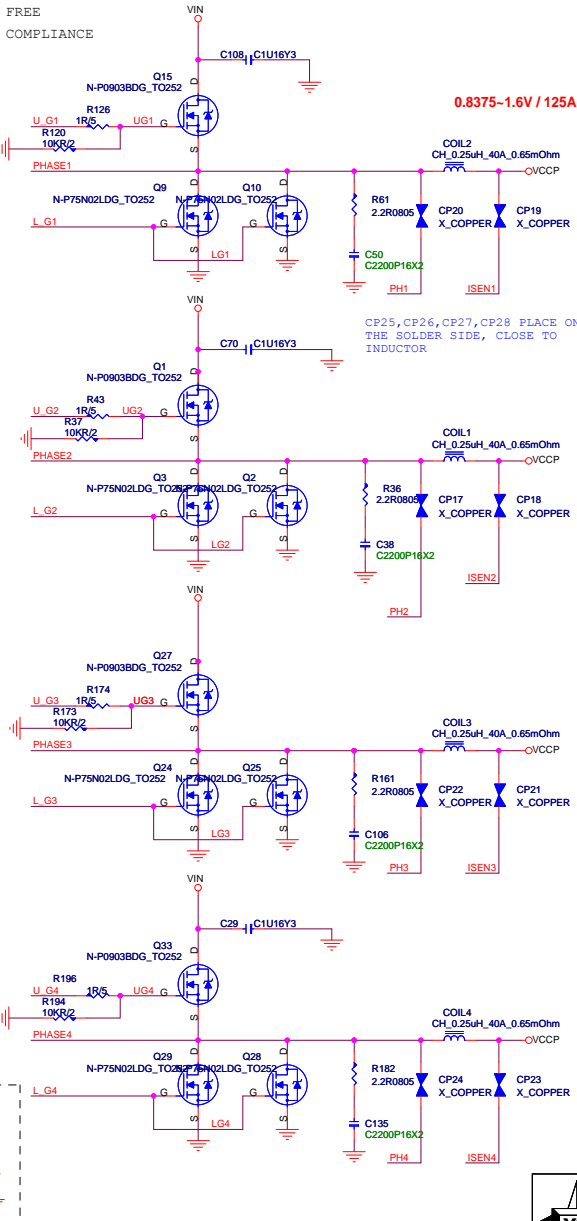
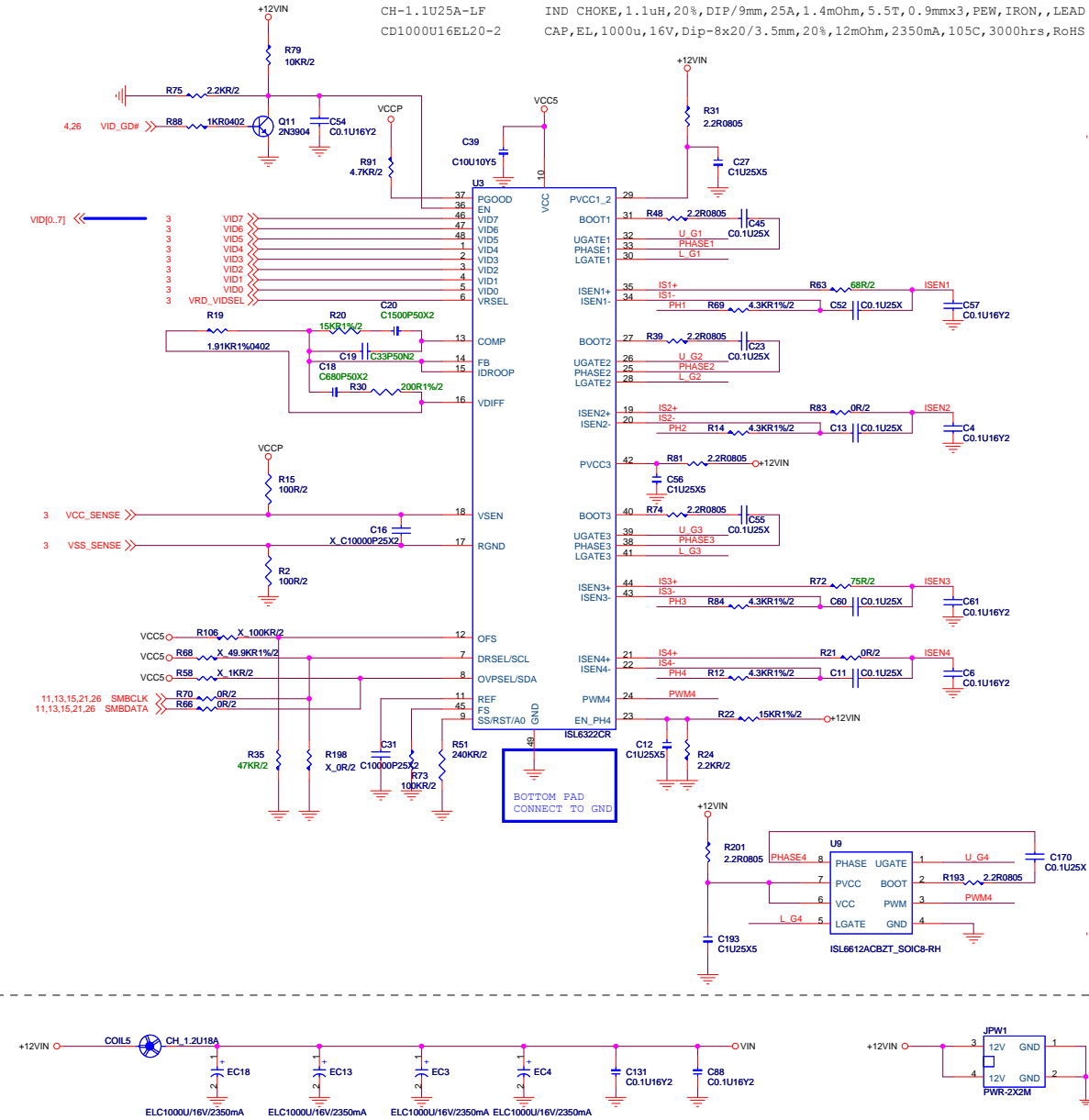


MICRO-STAR INT'L CO.,LTD

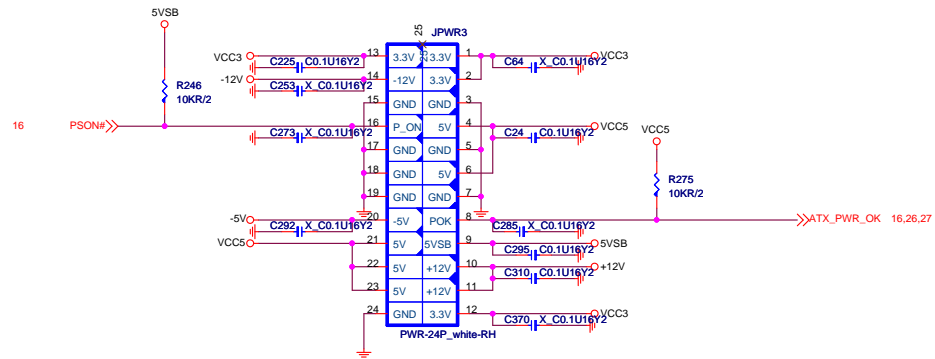
MS-7358

Size	Document Description	Rev
Custom	NB Core Power & DDR Power	3.1
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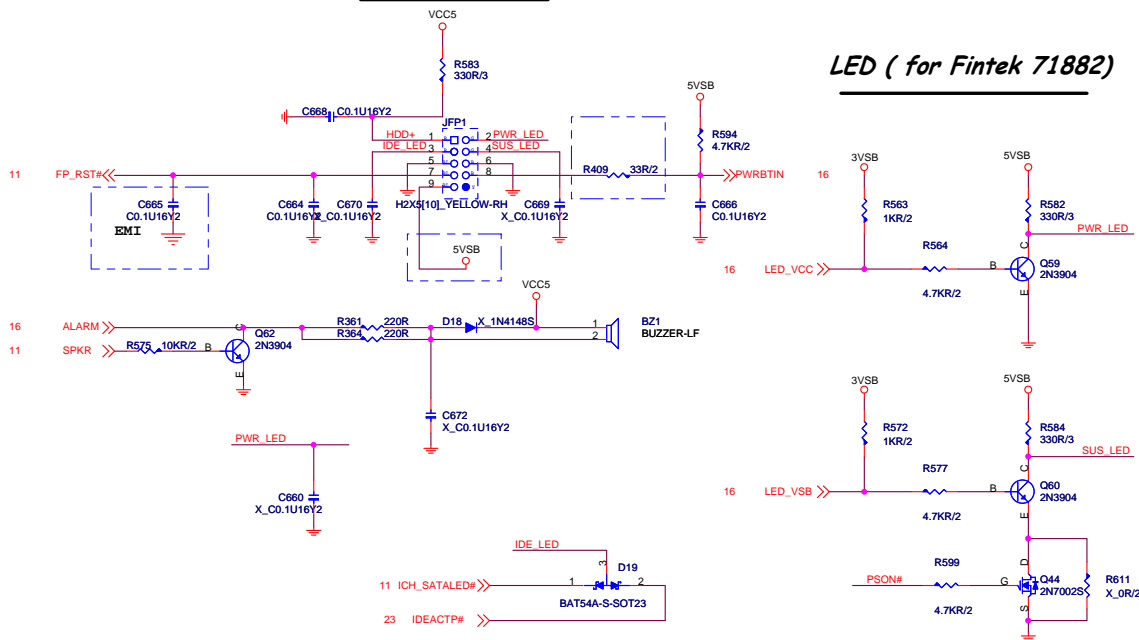
Voltage Regular Module



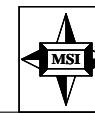
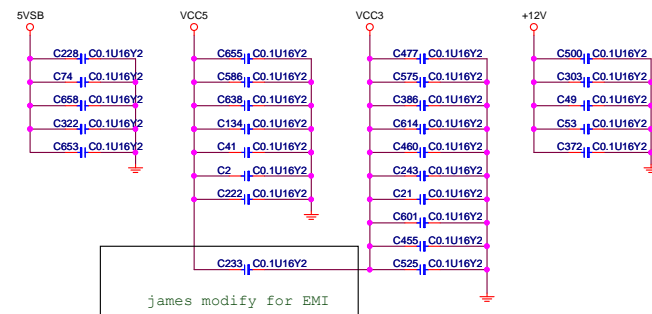
ATX POWER CONNECTOR



FRONT PANNEL



Cap. for EMI & Power



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Size	Document Description
Custom	ATX PWR-Connector & Front Panel

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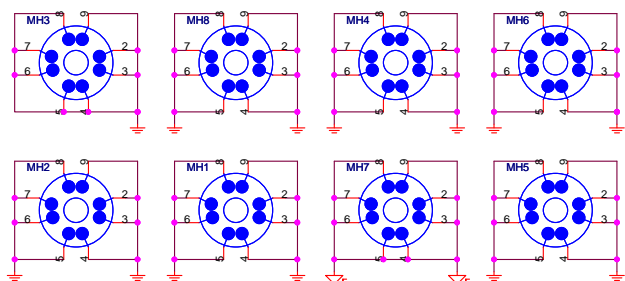
Optical Fiducial Marks-120



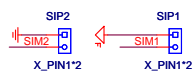
Optical Fiducial Marks-100



Mounting Holes



Simulation



7358-3.0

JFP2(4-6)



X_JUMPER-1X2A_green



BATTERY-CR2032

